RAIM'09 — October 27, 2009

Hardware Accelerator for the Tate Pairing based on Karatsuba Multipliers

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Joint work with:

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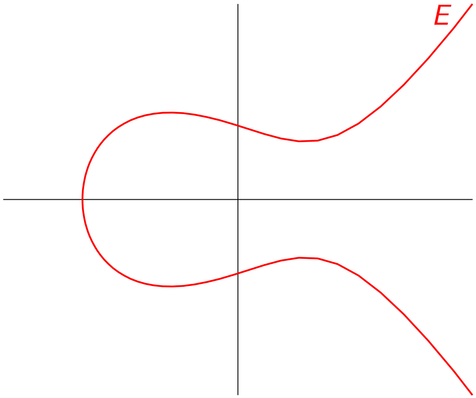
Nicolas Estibals	CACAO, LORIA, Nancy, France
Eiji Okamoto	LCIS, University of Tsukuba, Japan
Francisco Rodríguez-Henríquez	CINVESTAV-IPN, Mexico City, Mexico

Elliptic curves

- E defined by a Weierstraß equation of the form $y^2 = x^3 + Ax + B$



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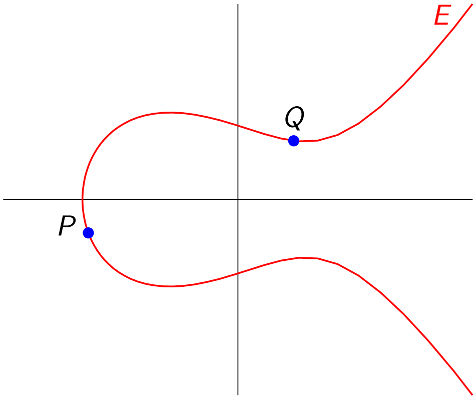

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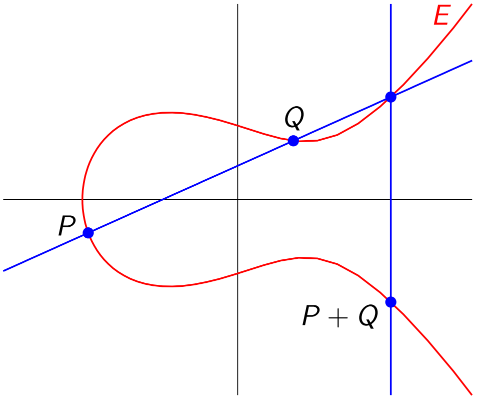

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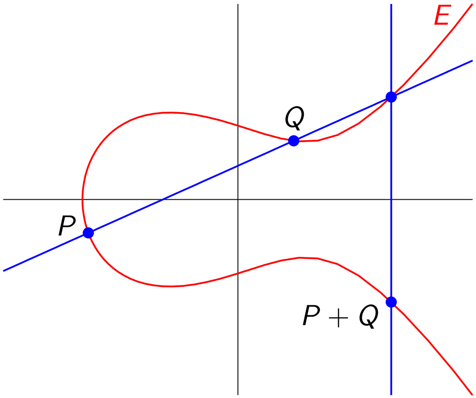

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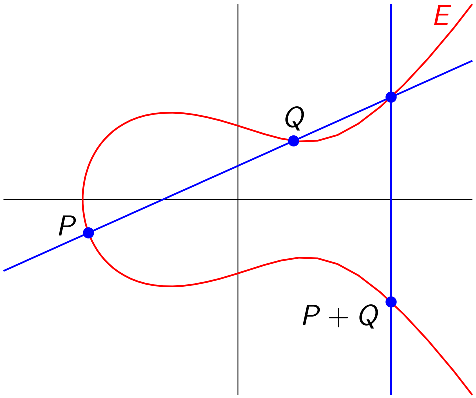
- But there's more: bilinear pairings



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- Pairing-based cryptography
- Hardware accelerator for the Tate pairing
- Implementation results
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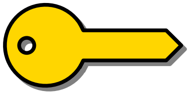

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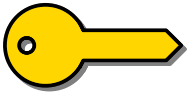

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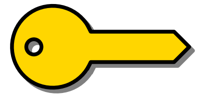

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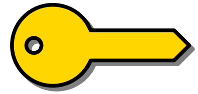

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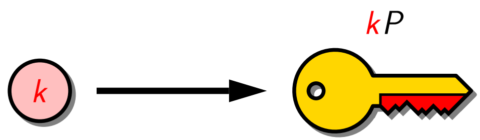

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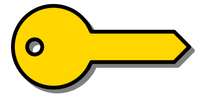

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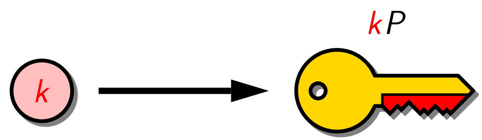

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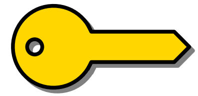

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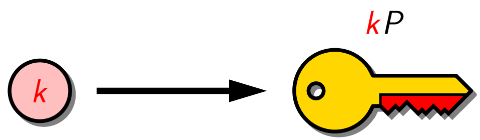

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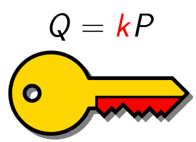

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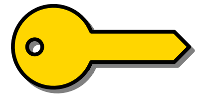

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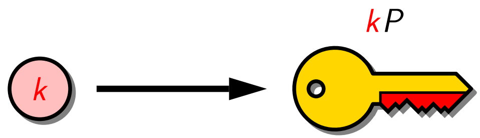

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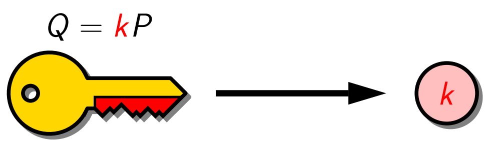

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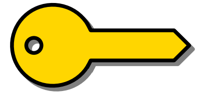

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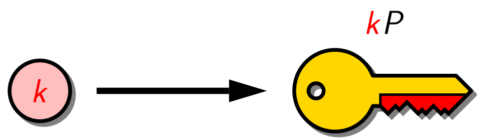

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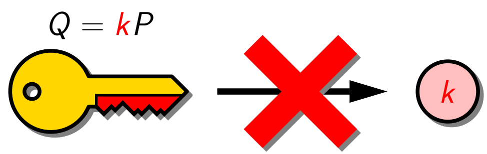

- We assume that the discrete logarithm problem (DLP) in $\mathbb{G}_1$ is hard

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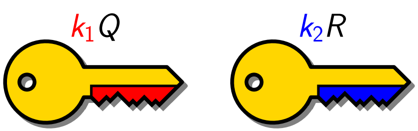

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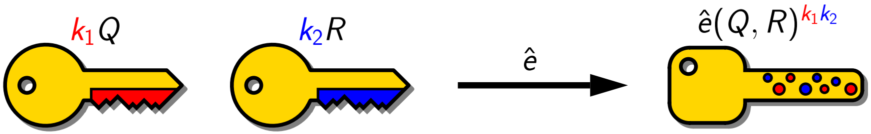

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$$\mathrm{DLP}_{\mathbb{G}_1}$$

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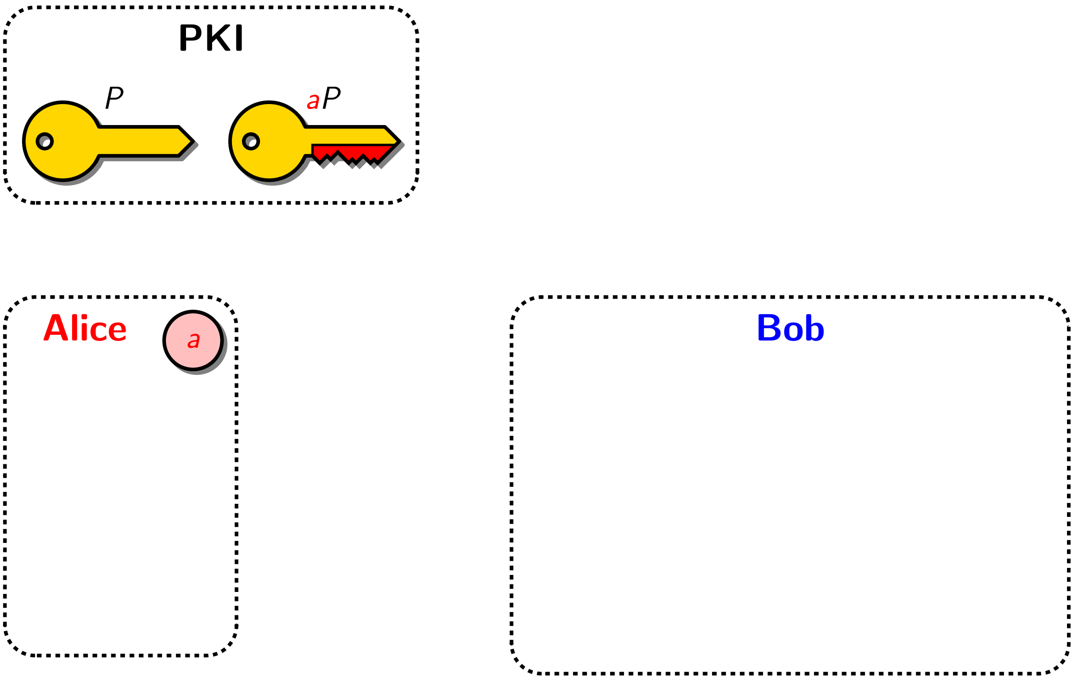
- One-round three-party key agreement (Joux, 2000)

- Identity-based encryption
  - Boneh–Franklin, 2001
  - Sakai–Kasahara, 2001

- Short digital signatures
  - Boneh–Lynn–Shacham, 2001
  - Zang–Safavi-Naini–Susilo, 2004

- ...

Short signature (Boneh, Lynn & Shacham, 2001)



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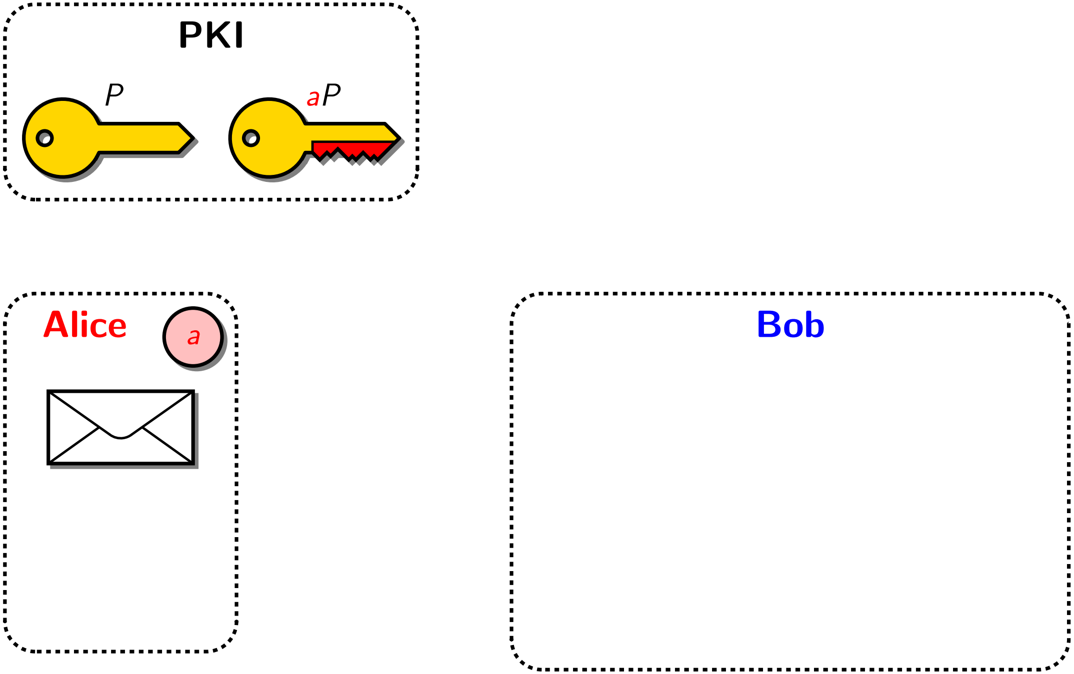

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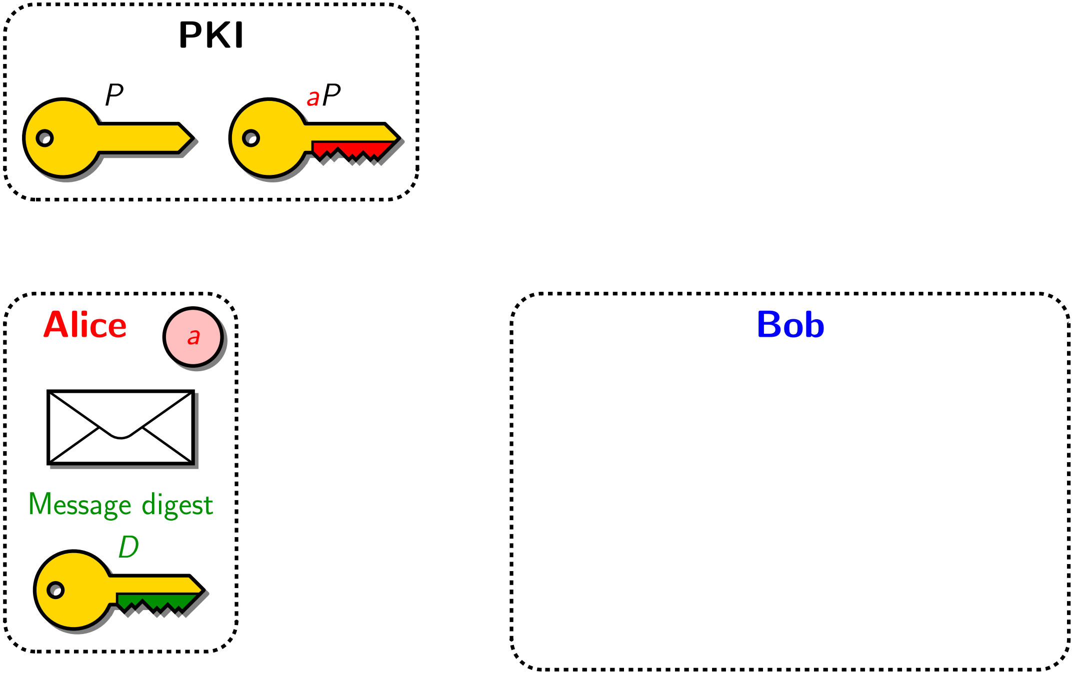

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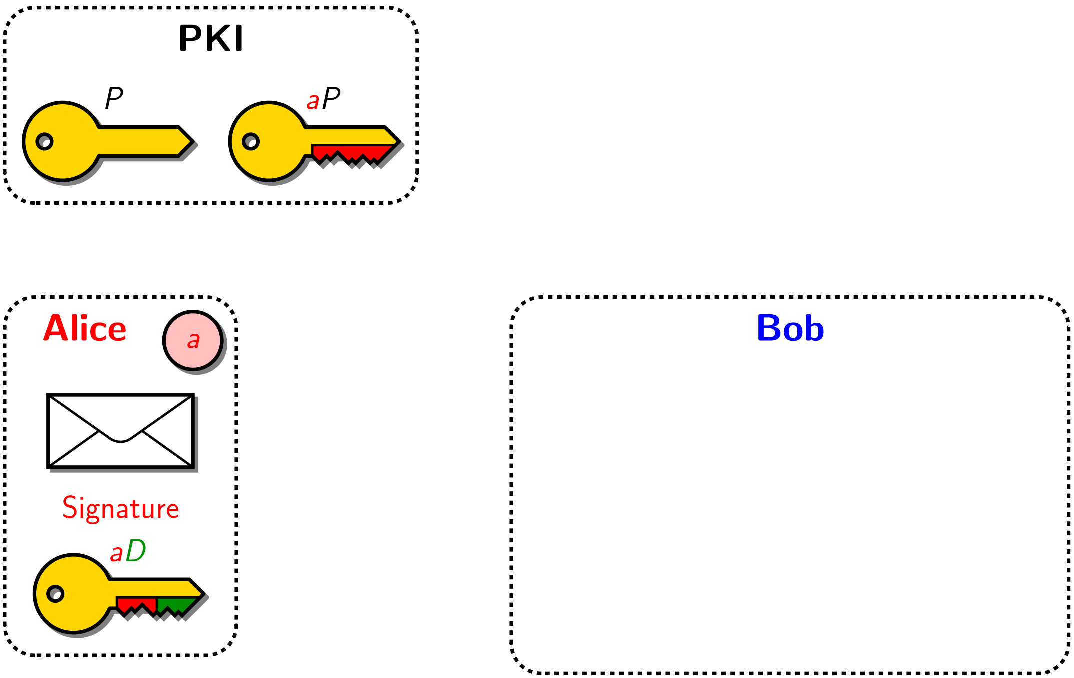

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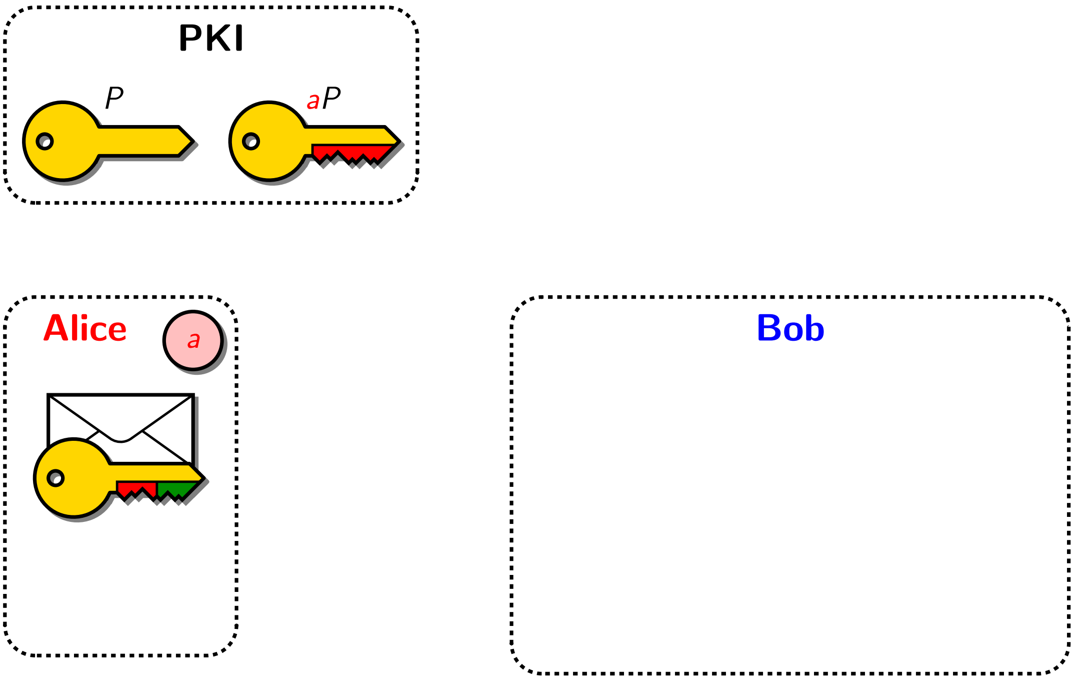

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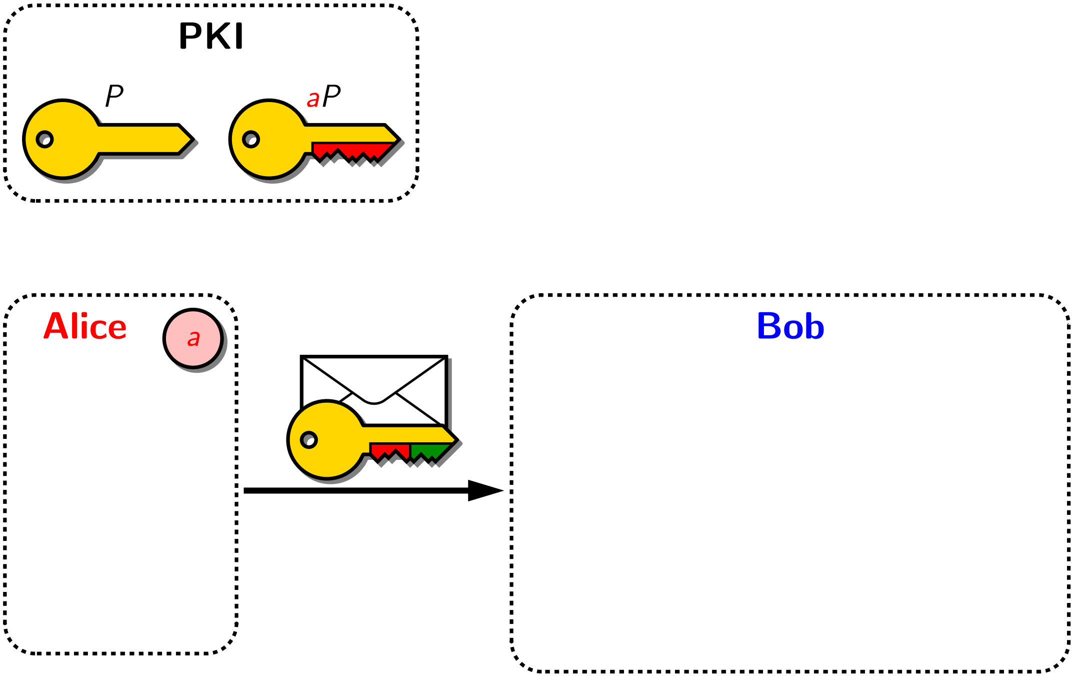

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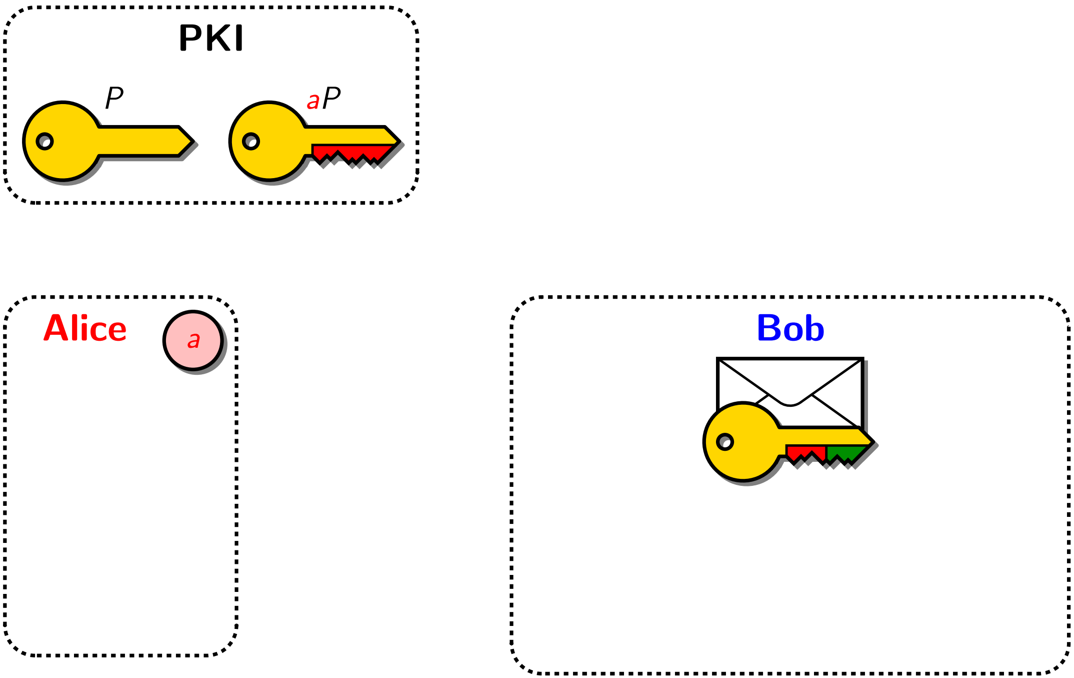

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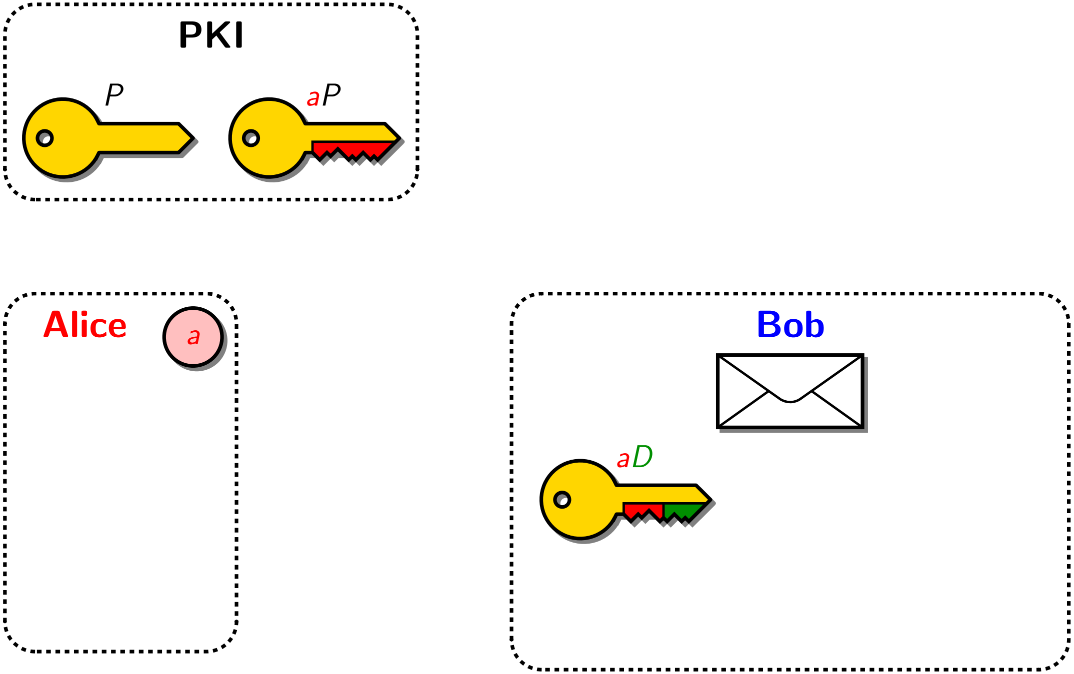

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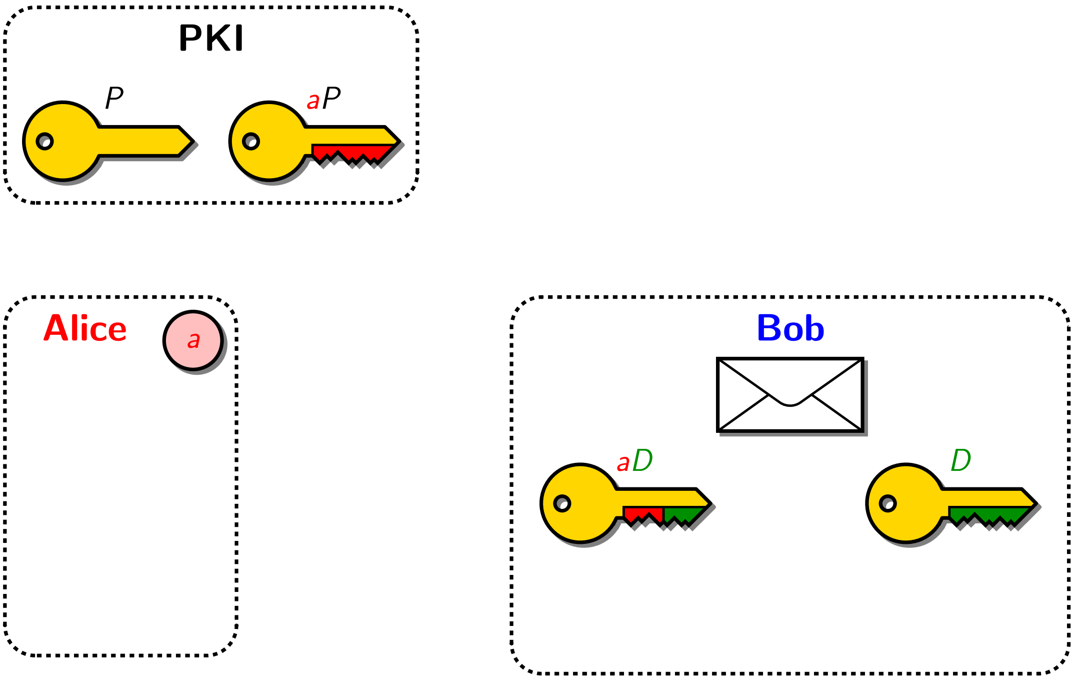

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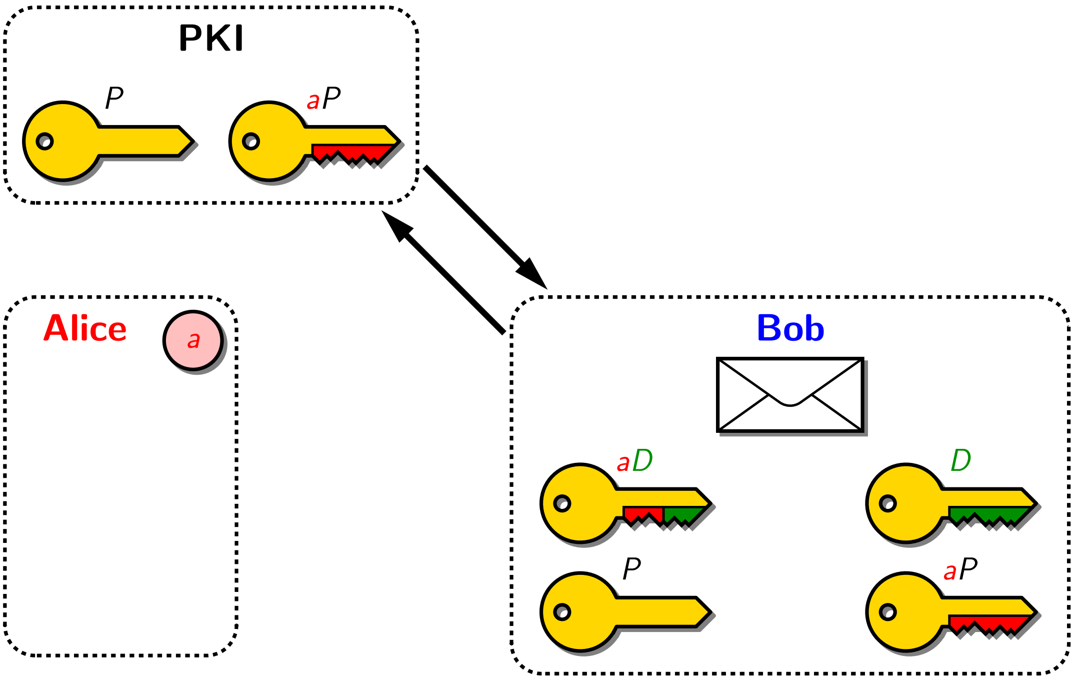

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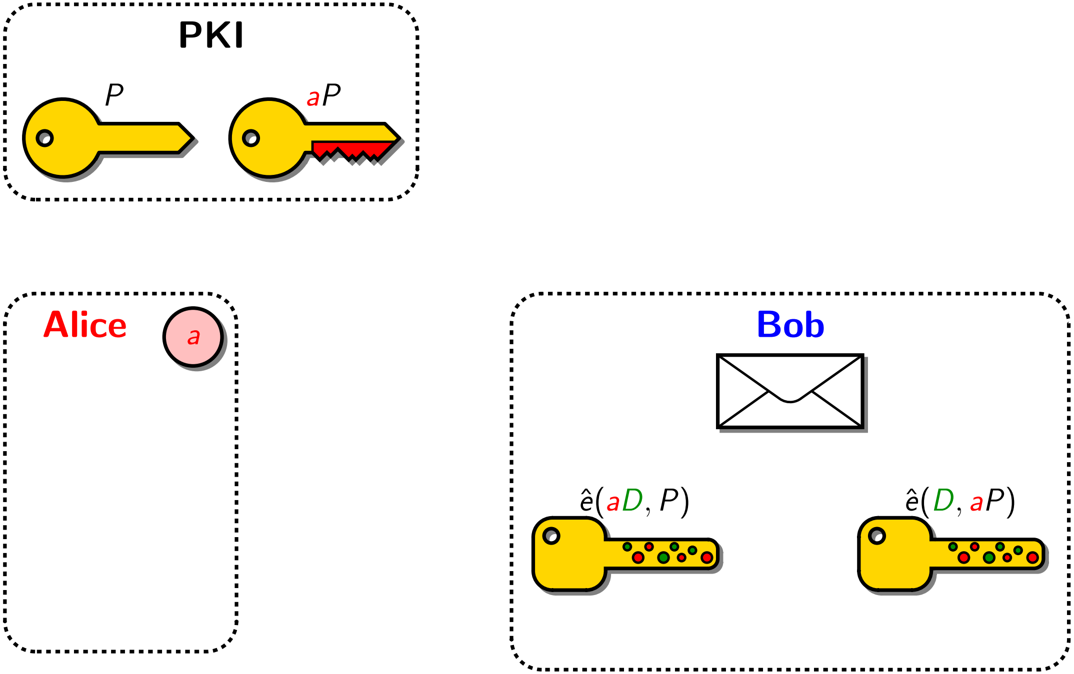

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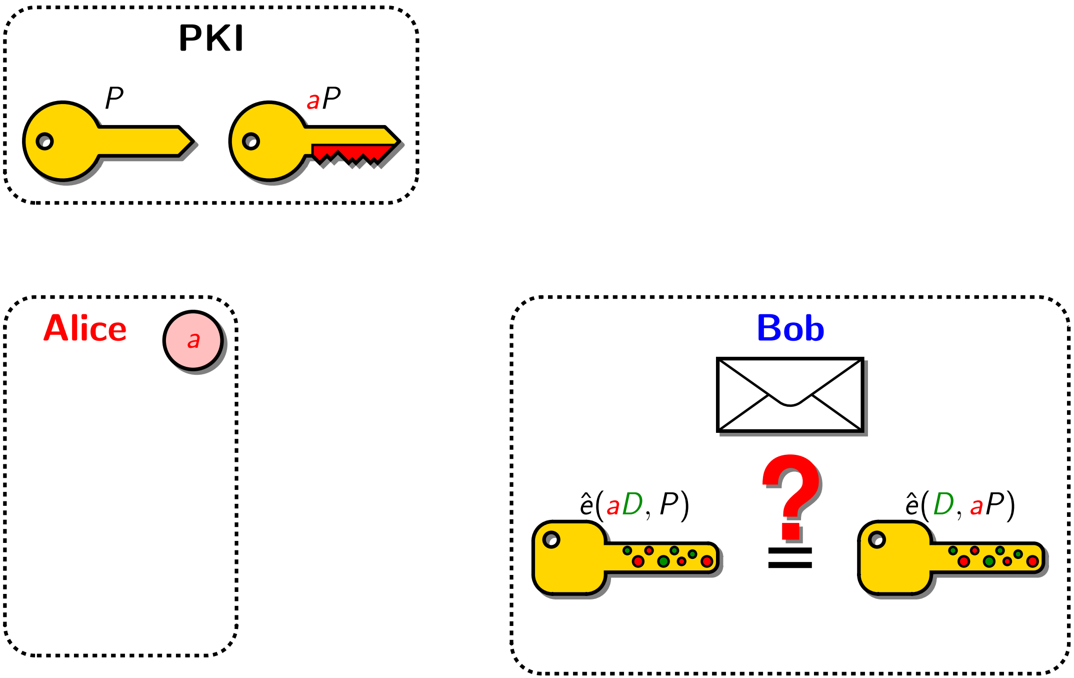

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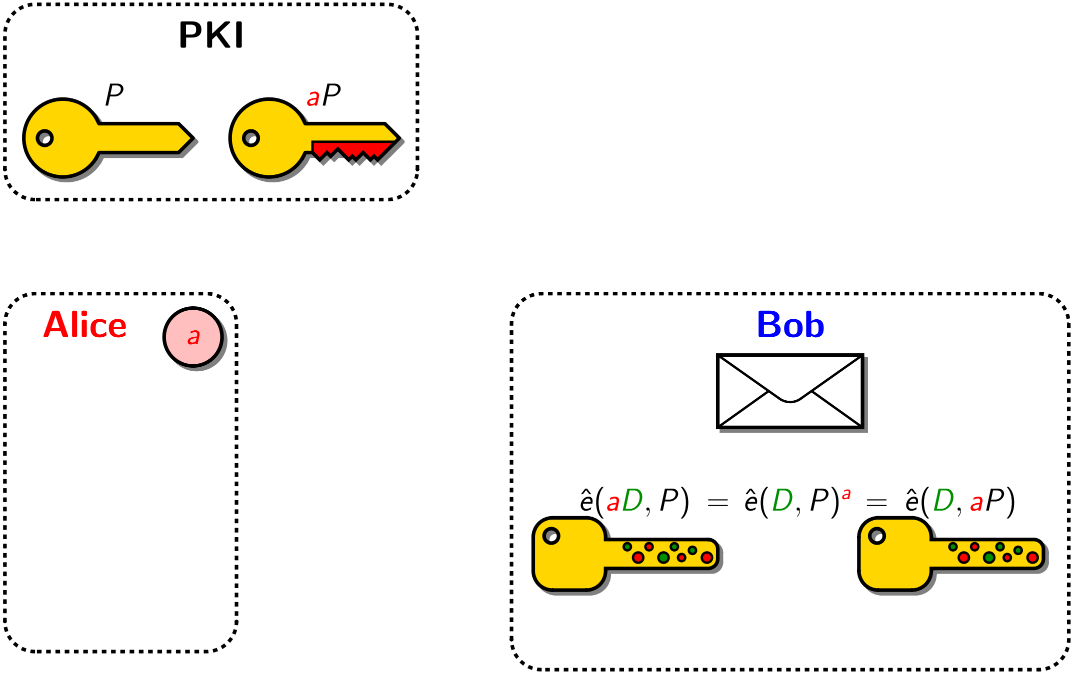

Context

$P \in \mathbb{G}_1$
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Bilinear pairing ê
$\hat{e}(P, Q) \in \mathbb{G}_2$

Context

- Reduced Tate pairing

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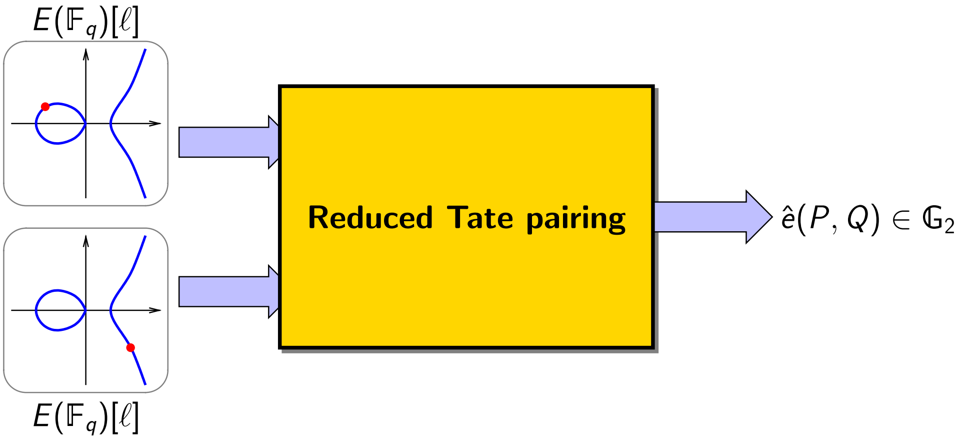

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  - input: two points P and Q in $E(\mathbb{F}_q)[\ell]$

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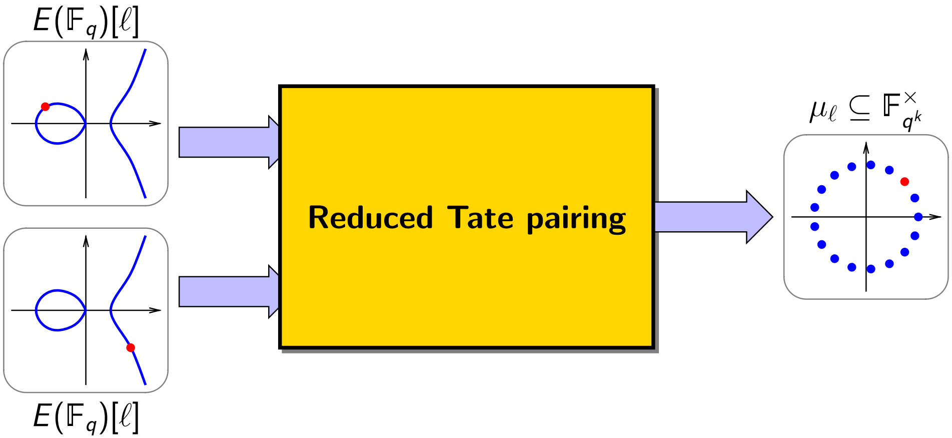

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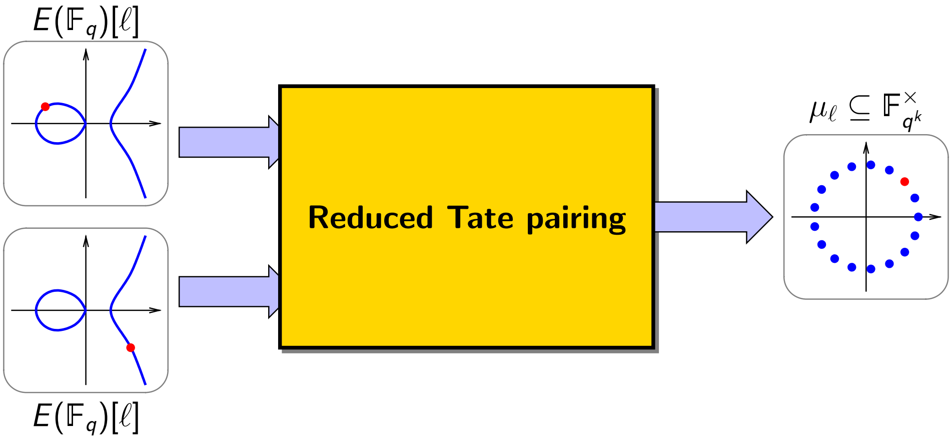

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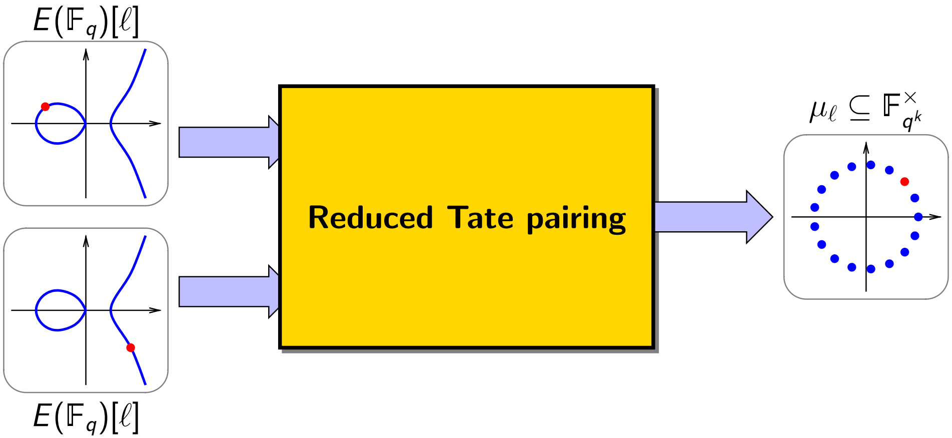

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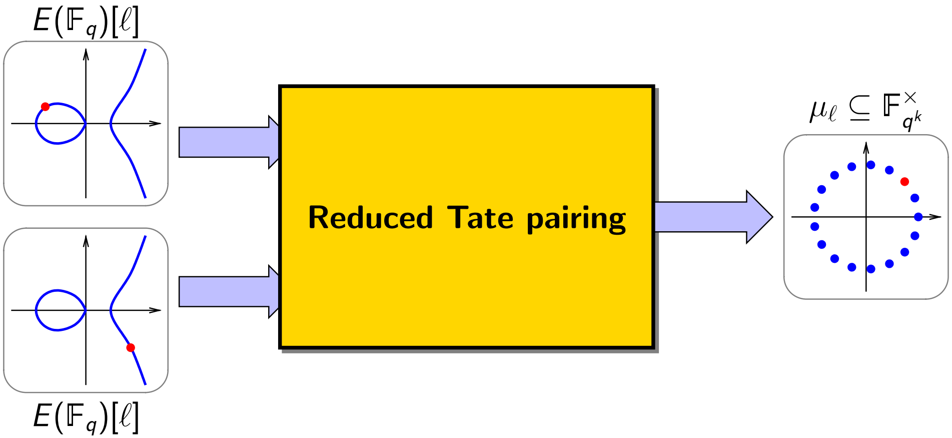
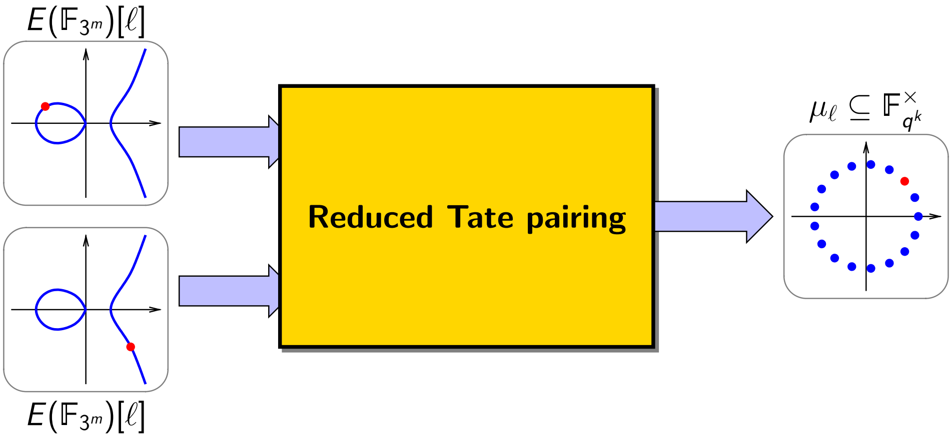
- Which elliptic curves? Supersingular curves
  - easier arithmetic on the curve
  - lower security

Context



- Reduced Tate pairing
  - input: two points P and Q in $E(\mathbb{F}_q)[\ell]$
  - output: an ℓ-th root of unity in the extension $\mathbb{F}_{q^k}^\times$
- Which elliptic curves? Supersingular curves
  - easier arithmetic on the curve
  - lower security $\Rightarrow$ characteristic 3 ($k = 6$)

Context



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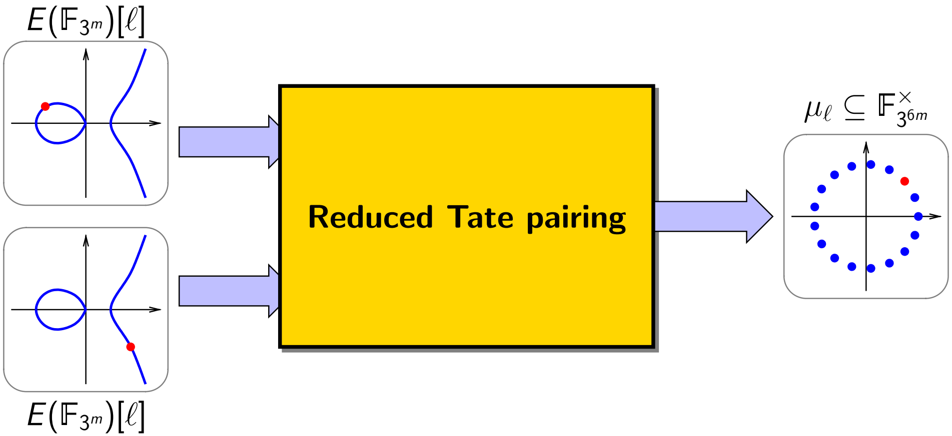

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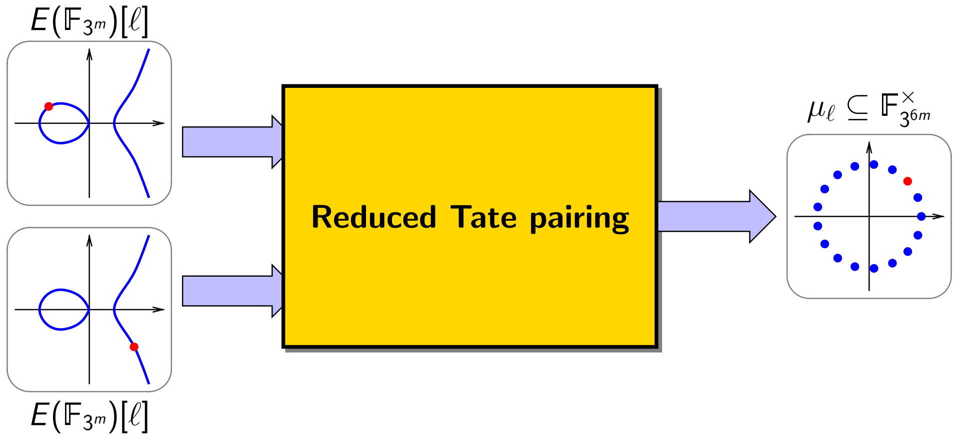

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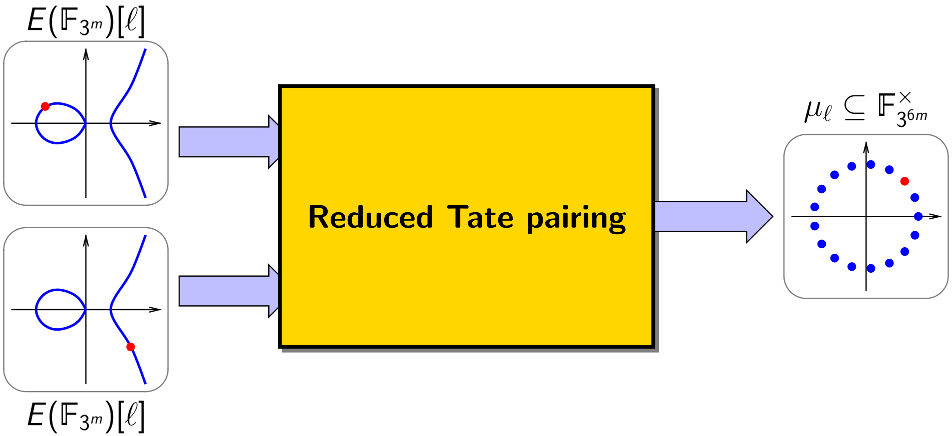

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Outline of the talk

- Pairing-based cryptography
- Hardware accelerator for the Tate pairing
- Implementation results
- Concluding thoughts

Reduced Tate pairing

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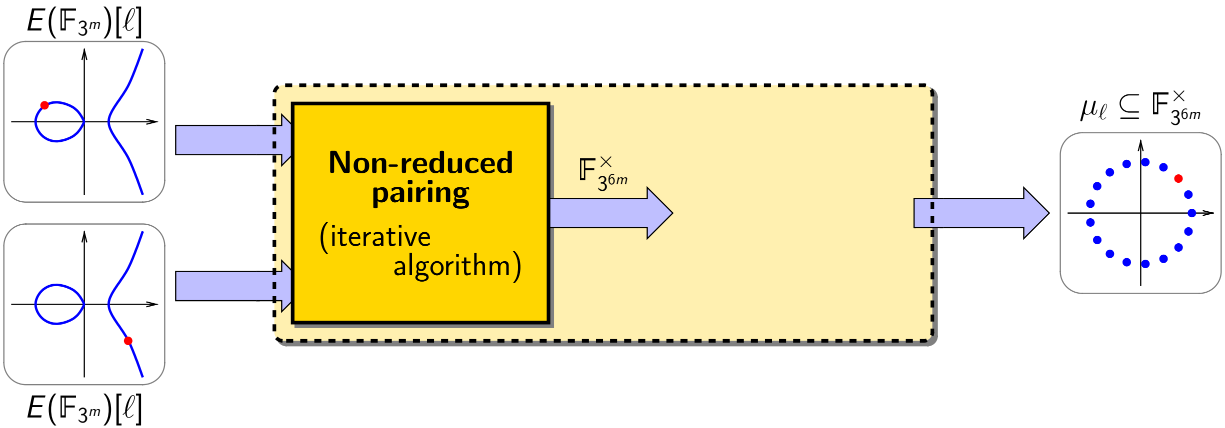
- Two very different steps

Reduced Tate pairing



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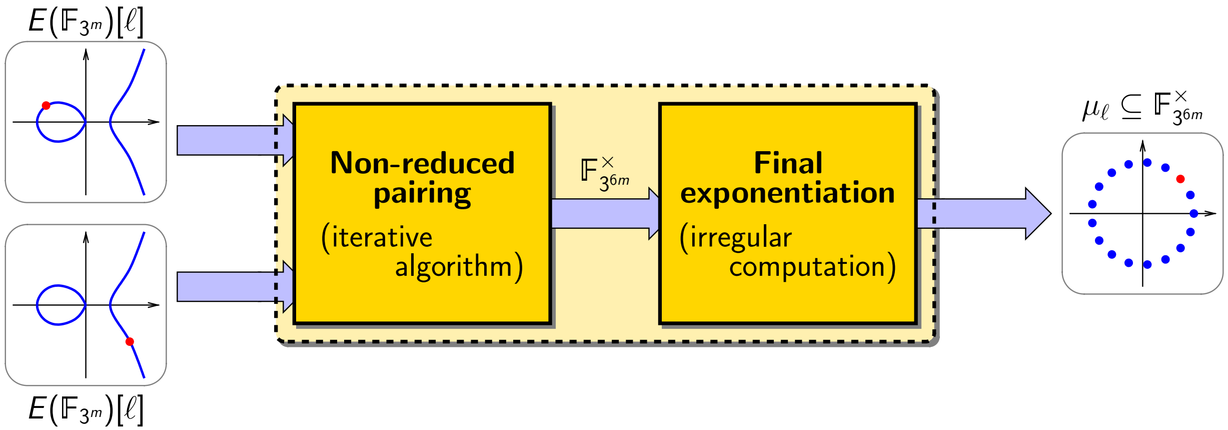

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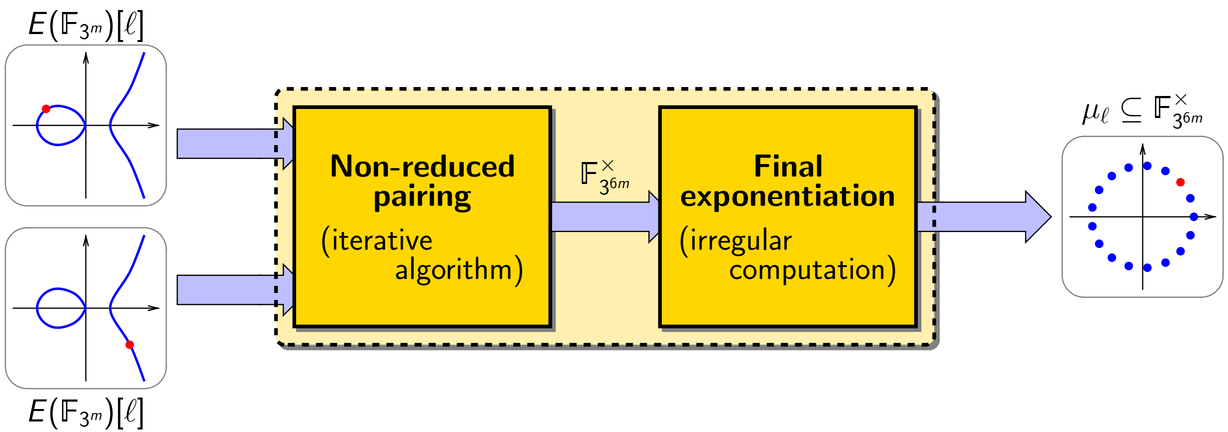
Reduced Tate pairing



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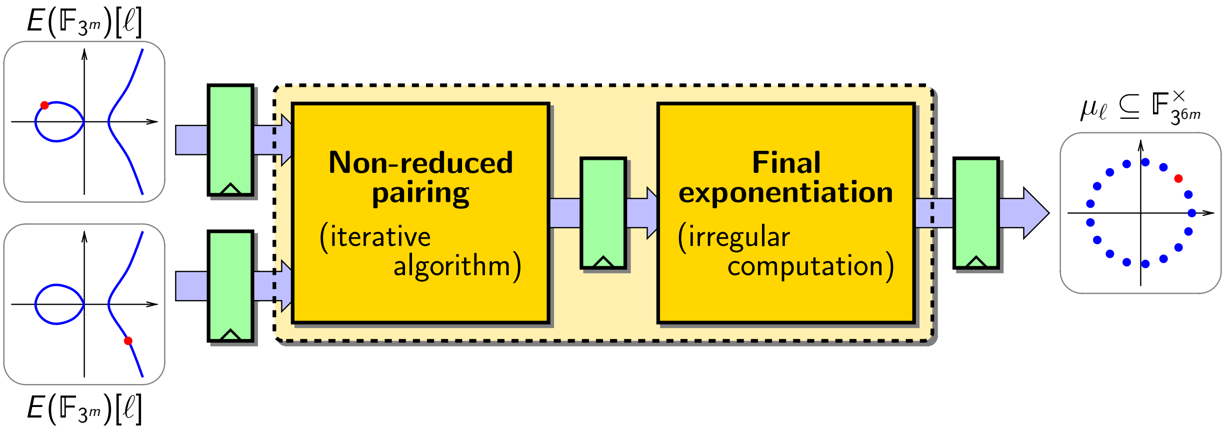
- Idea: use two distinct coprocessors

Reduced Tate pairing



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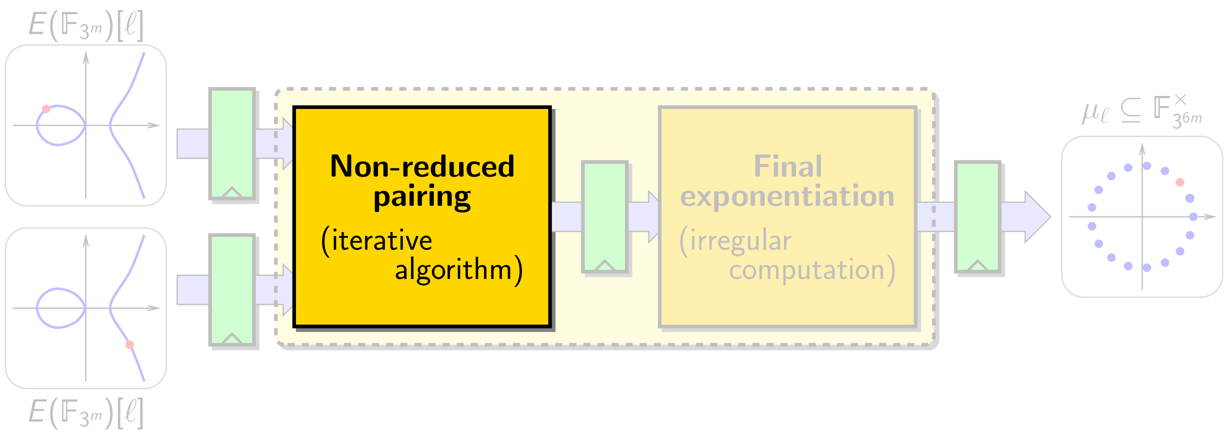

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Computing the non-reduced pairing

- η_T pairing: shorter loop

for $i \leftarrow 0$ **to** $(m-1)/2$ **do**

end for

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- Based on Miller's algorithm:

for $i \leftarrow 0$ **to** $(m-1)/2$ **do**

$$x_P \leftarrow \sqrt[3]{x_P} \quad ; \quad y_P \leftarrow \sqrt[3]{y_P}$$
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$$t \leftarrow x_P + x_Q \qquad u \leftarrow y_P y_Q$$
$$S \leftarrow -t^2 \pm u\sigma - t\rho - \rho^2$$

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- Fully parallel, pipelined multiplier over $\mathbb{F}_{3^m}$

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- Sparse multiplication over $\mathbb{F}_{3^{6m}}$
  - $12\times$ and $59+$ over $\mathbb{F}_{3^m}$ (Gorla *et al.*, SAC 2007)

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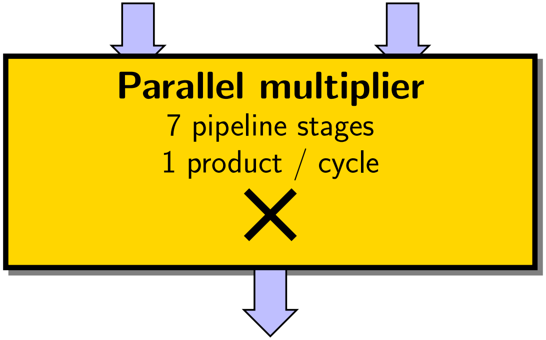
- Objective: keep the multiplier pipeline busy
  - 7-stage pipeline
  - one product per cycle
  - 17 cycles per iteration

Coprocessor for the non-reduced pairing



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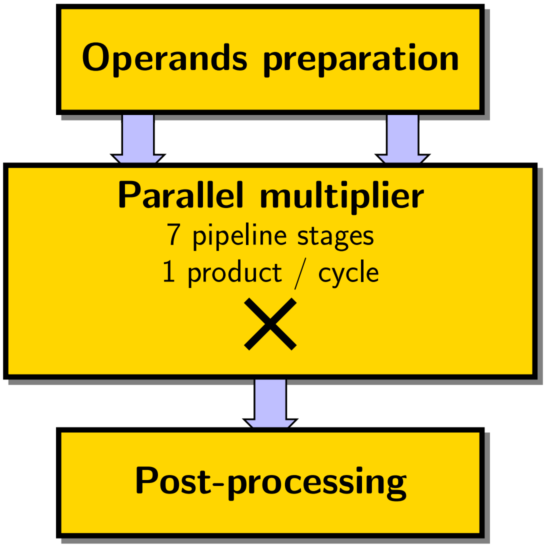

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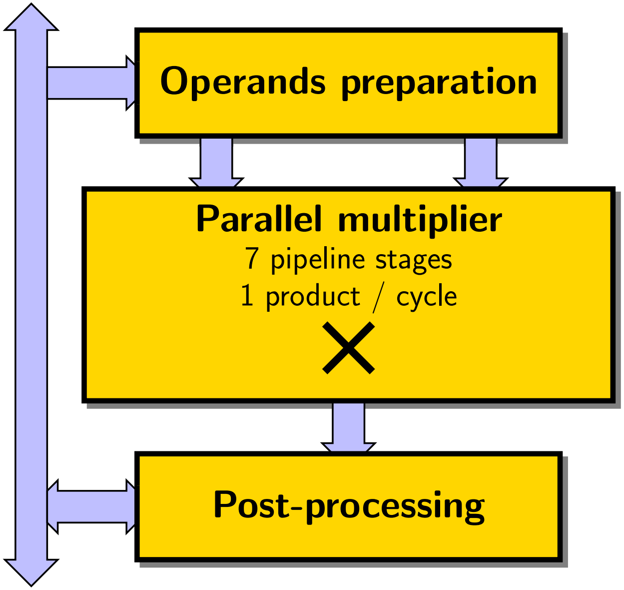

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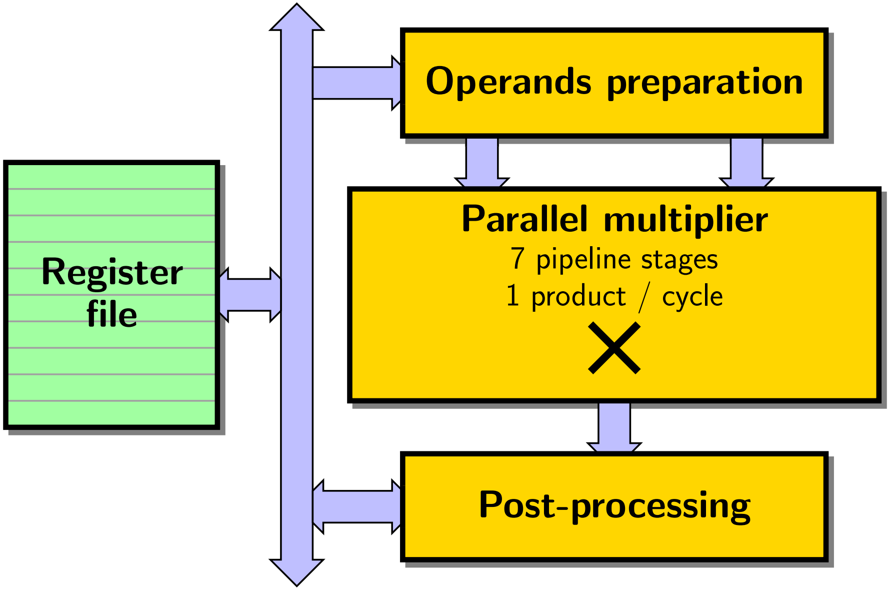

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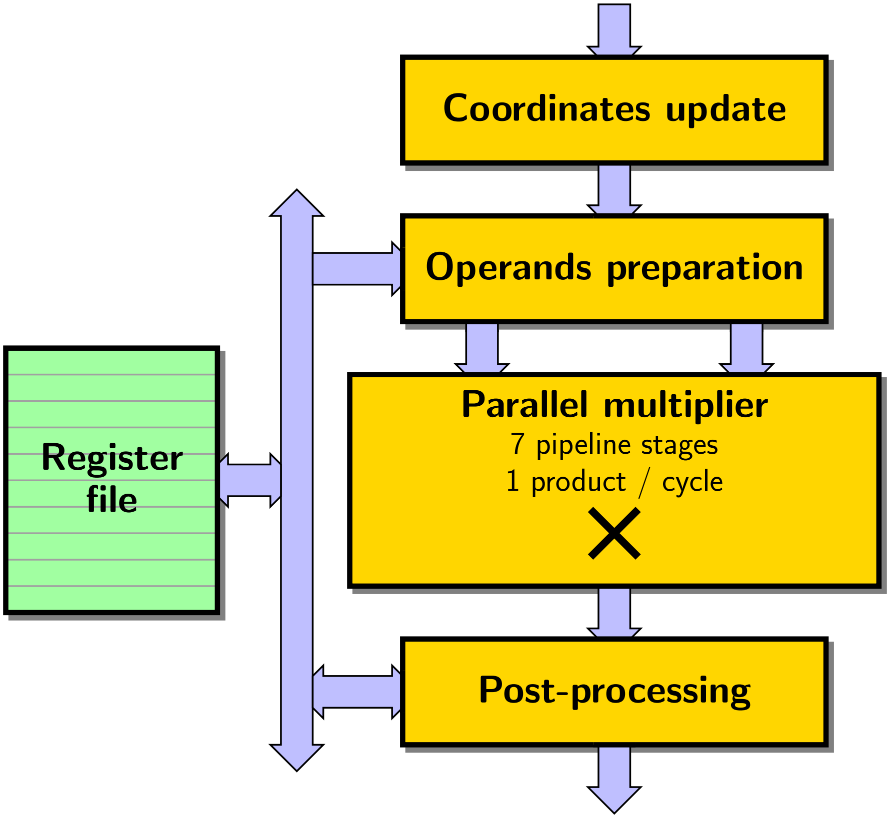

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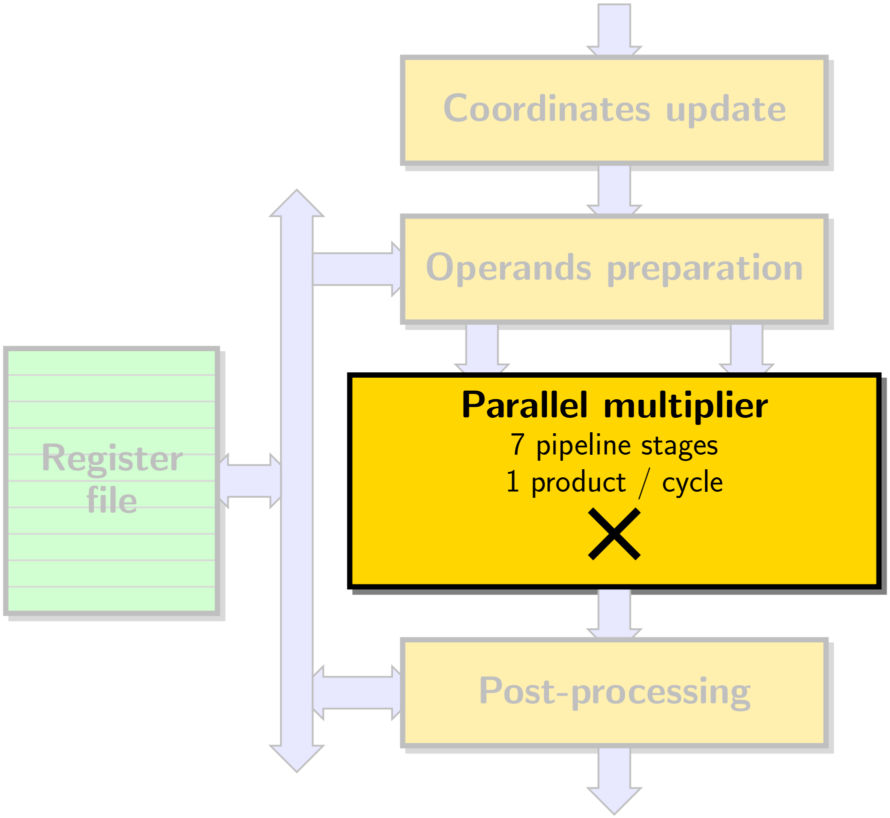

Our parallel multiplier

- Polynomial basis:

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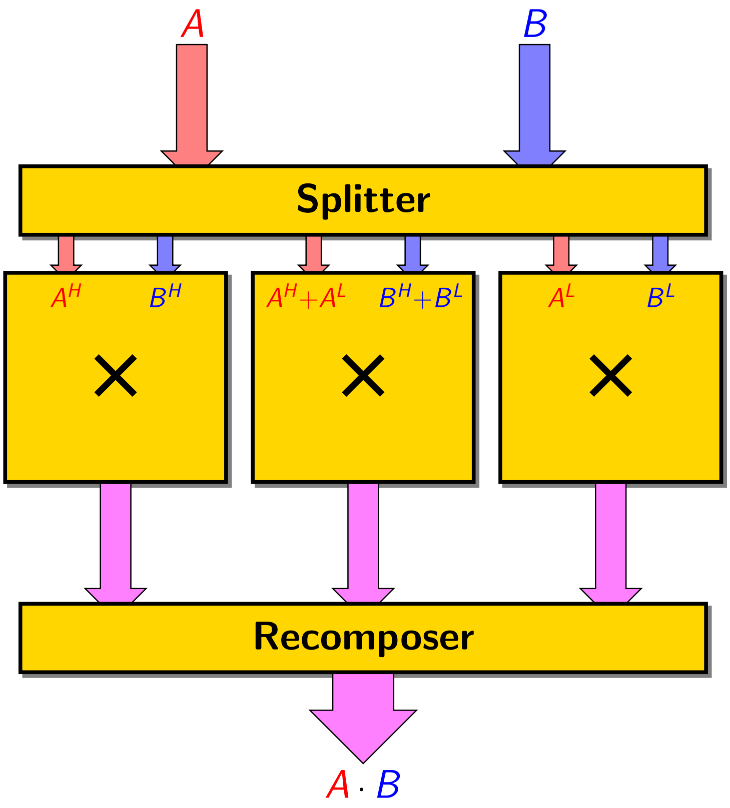

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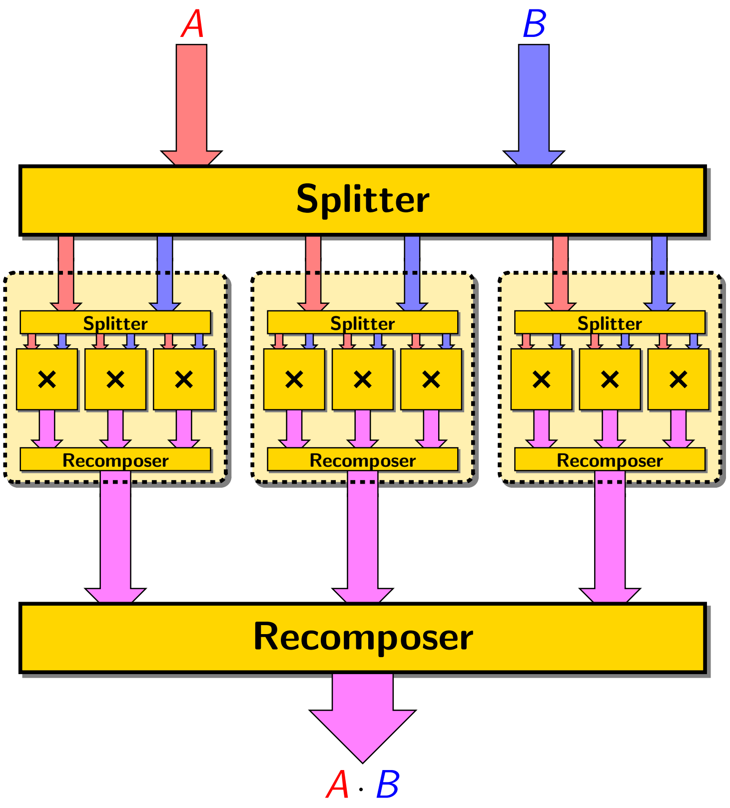

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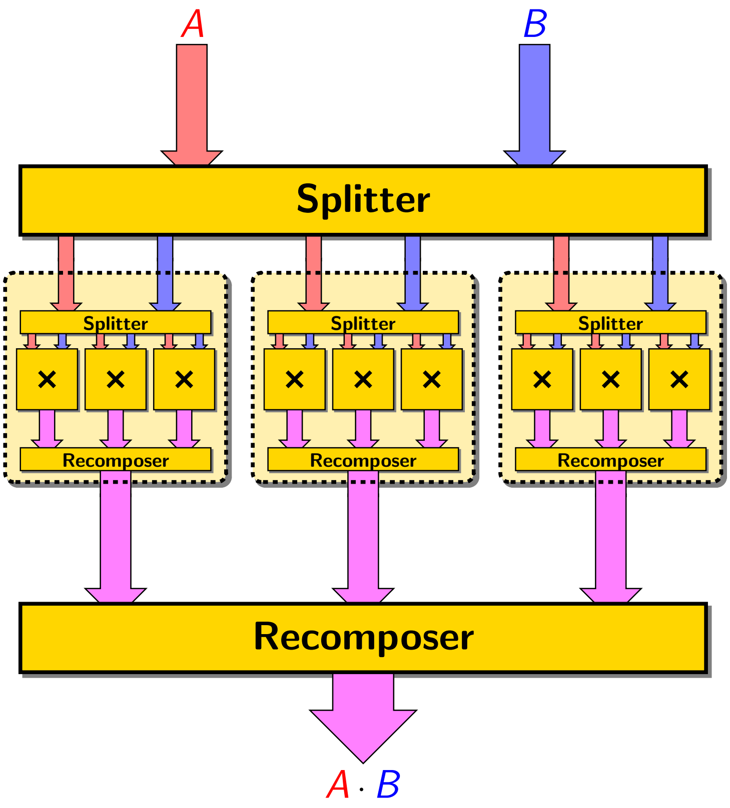
  - select the best method for each stage



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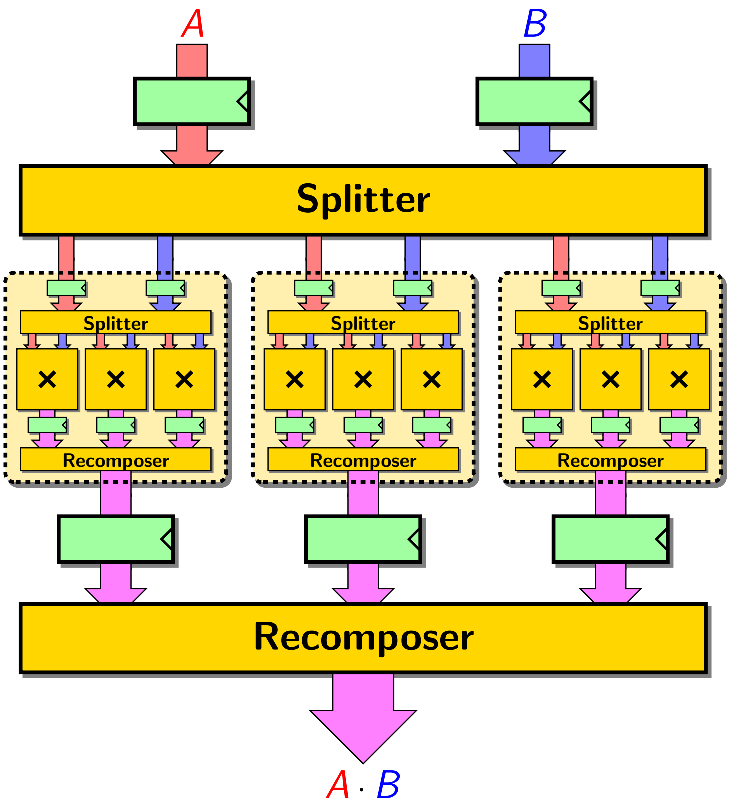

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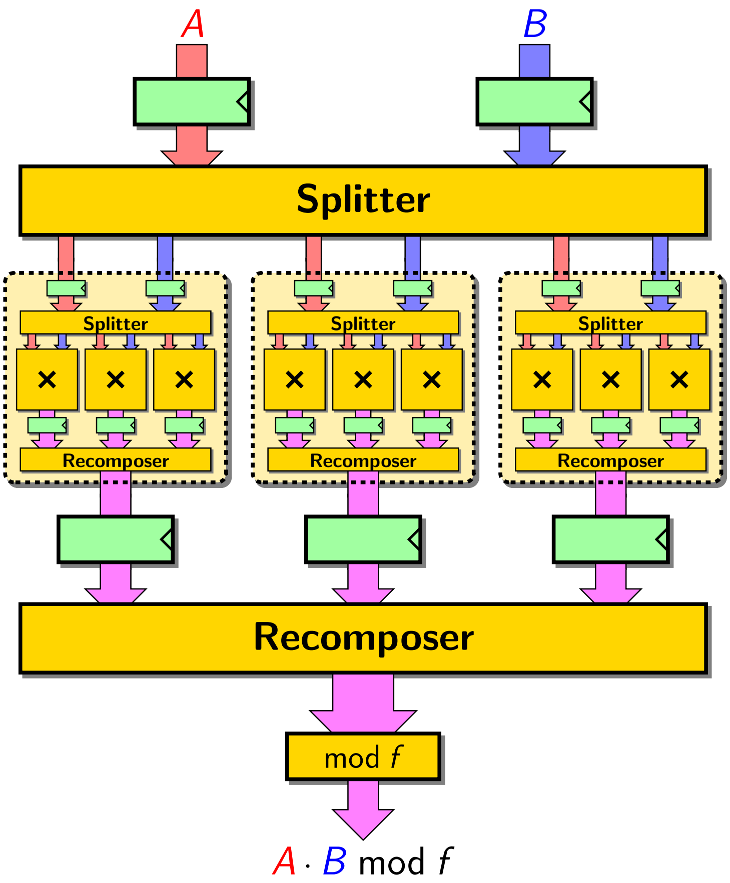
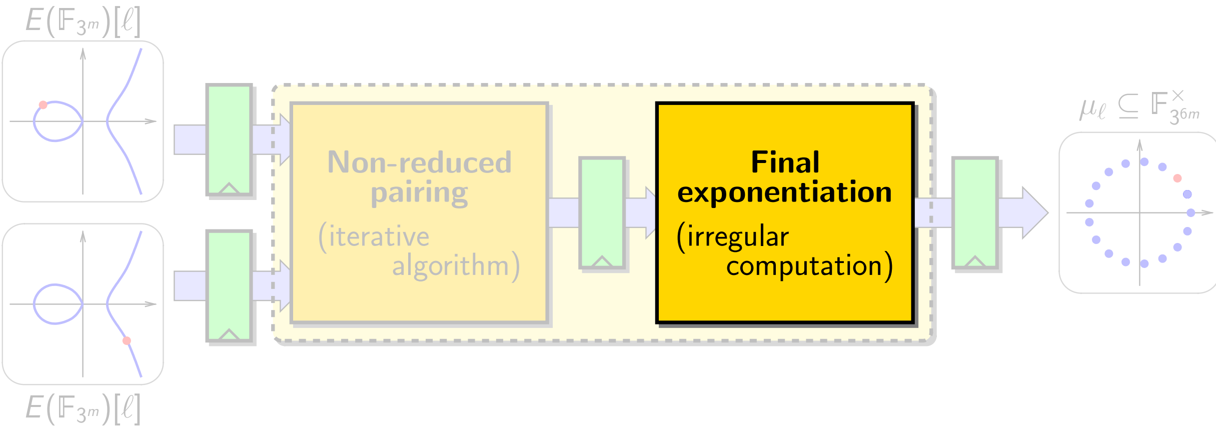
- Final reduction modulo f



Final exponentiation



- Design rationale:
  - as small as possible
  - at least as fast as the computation of the non-reduced pairing

Coprocessor for the final exponentiation

- Highly sequential computation
- Very heterogeneous

Coprocessor for the final exponentiation

$$\left.\begin{array}{l}\blacktriangleright\ \text{Highly sequential computation} \\[1em] \blacktriangleright\ \text{Very heterogeneous}\end{array}\right\} \Rightarrow \begin{array}{c}\text{general-purpose} \\ \text{finite-field arithmetic} \\ \text{processor}\end{array}$$

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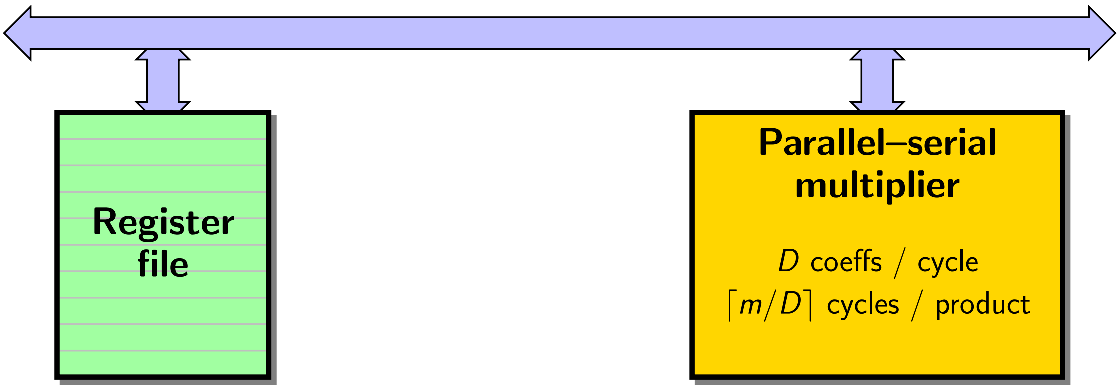

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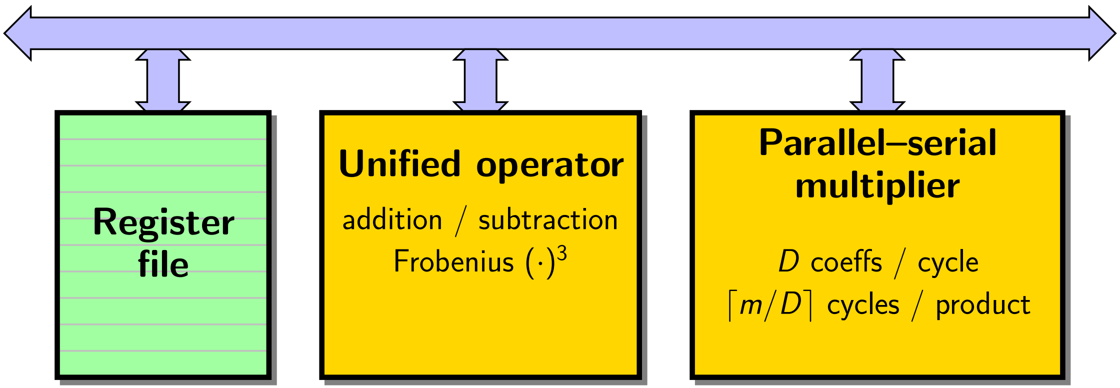

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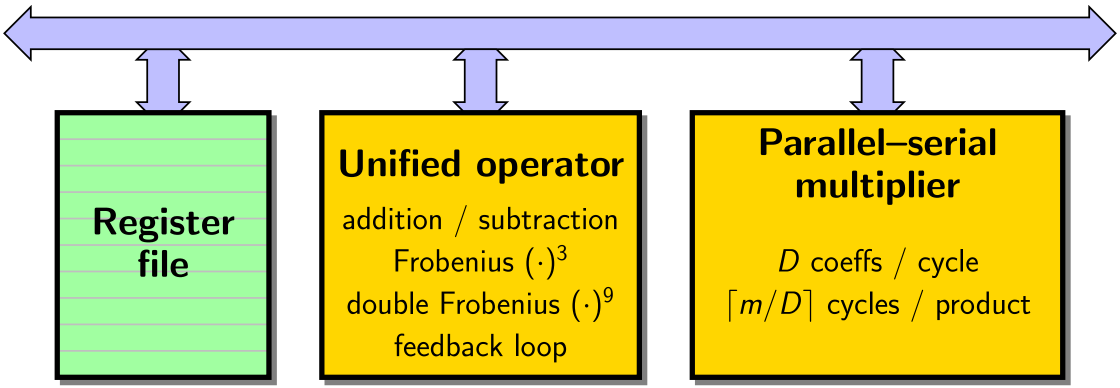

Outline of the talk

- Pairing-based cryptography
- Hardware accelerator for the Tate pairing
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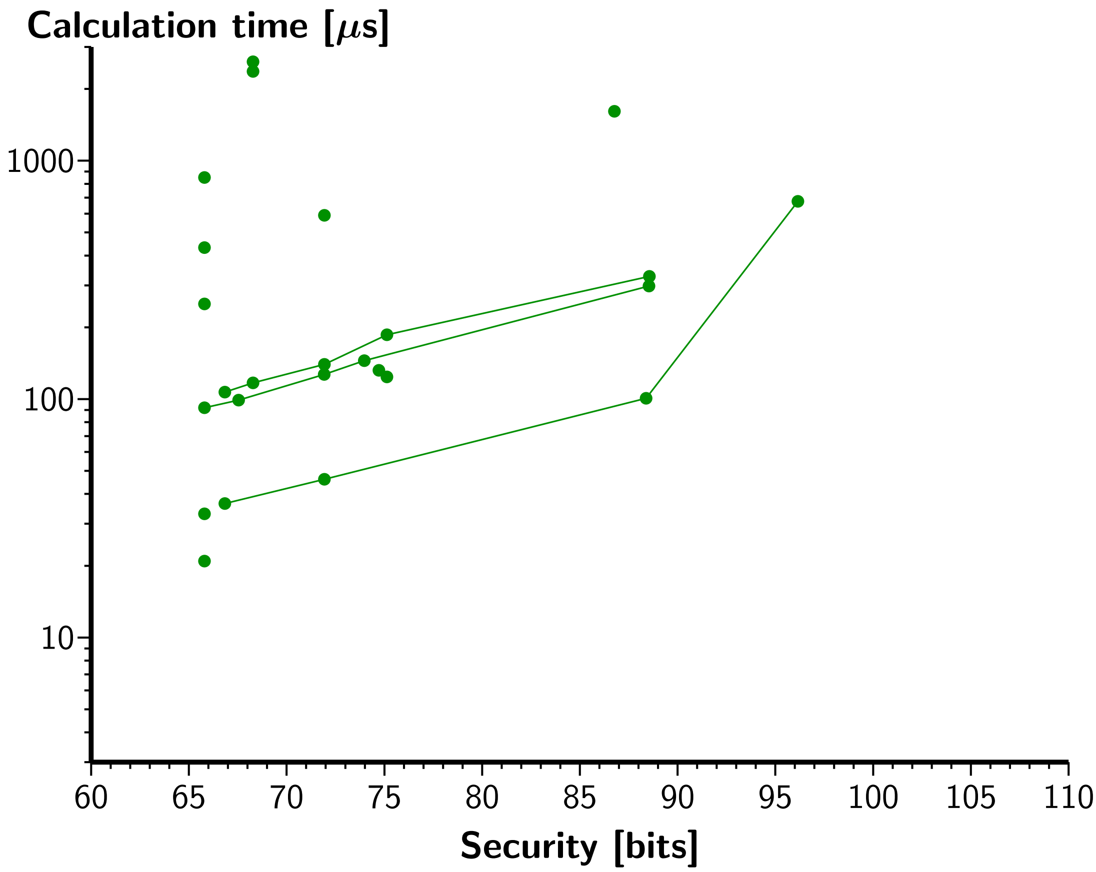
Experimental setup

- Full Tate pairing computation:
  - non-reduced pairing and
  - final exponentiation
- Prototyped on Xilinx Virtex-II Pro and Virtex-4 LX FPGAs
- Post–place-and-route timing and area estimations


Calculation time [μs]
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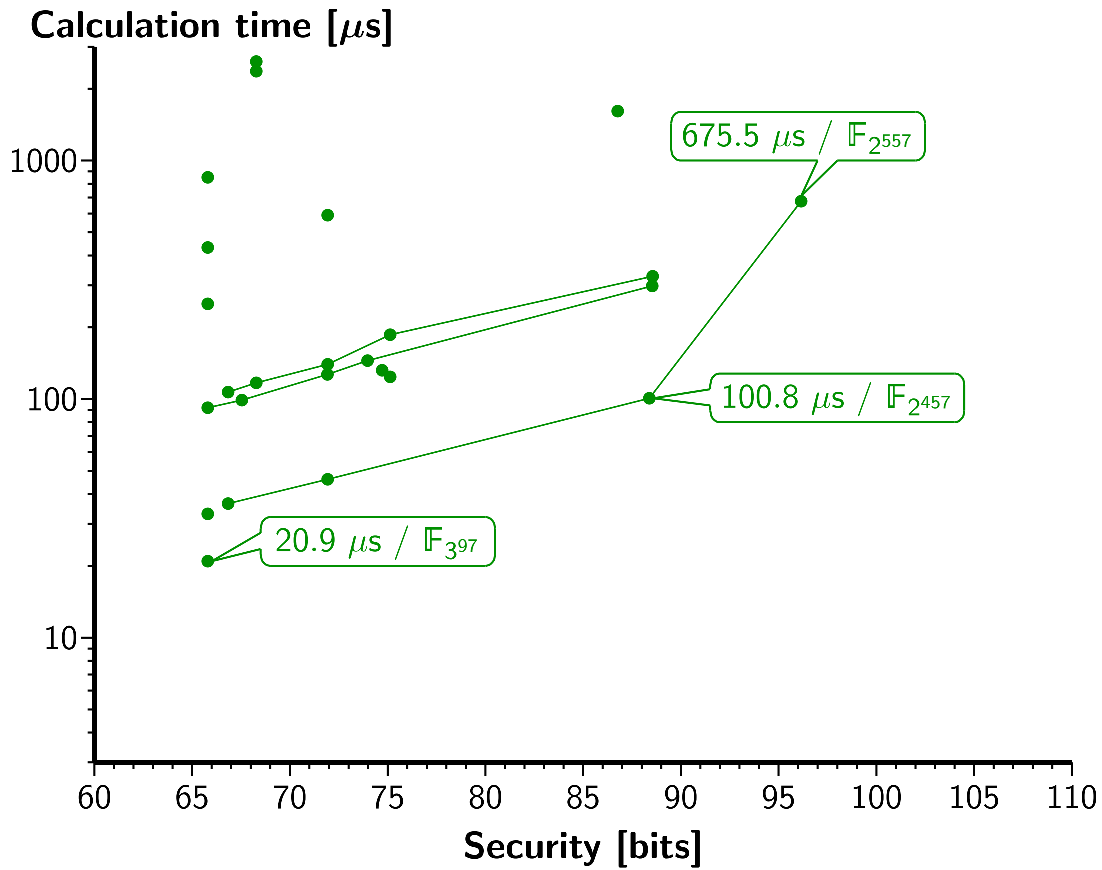
Security [bits]


Calculation time [μs]
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675.5 μs / $\mathbb{F}_{2^{557}}$
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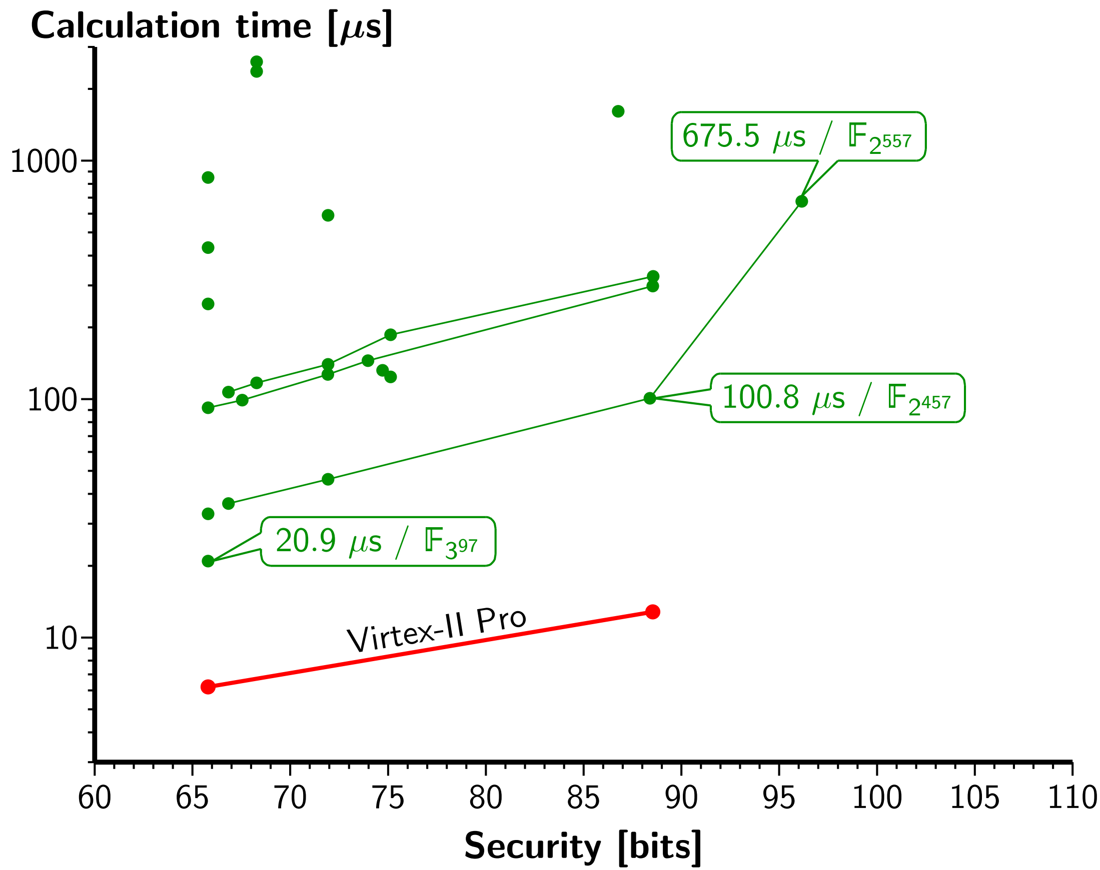

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Virtex-II Pro
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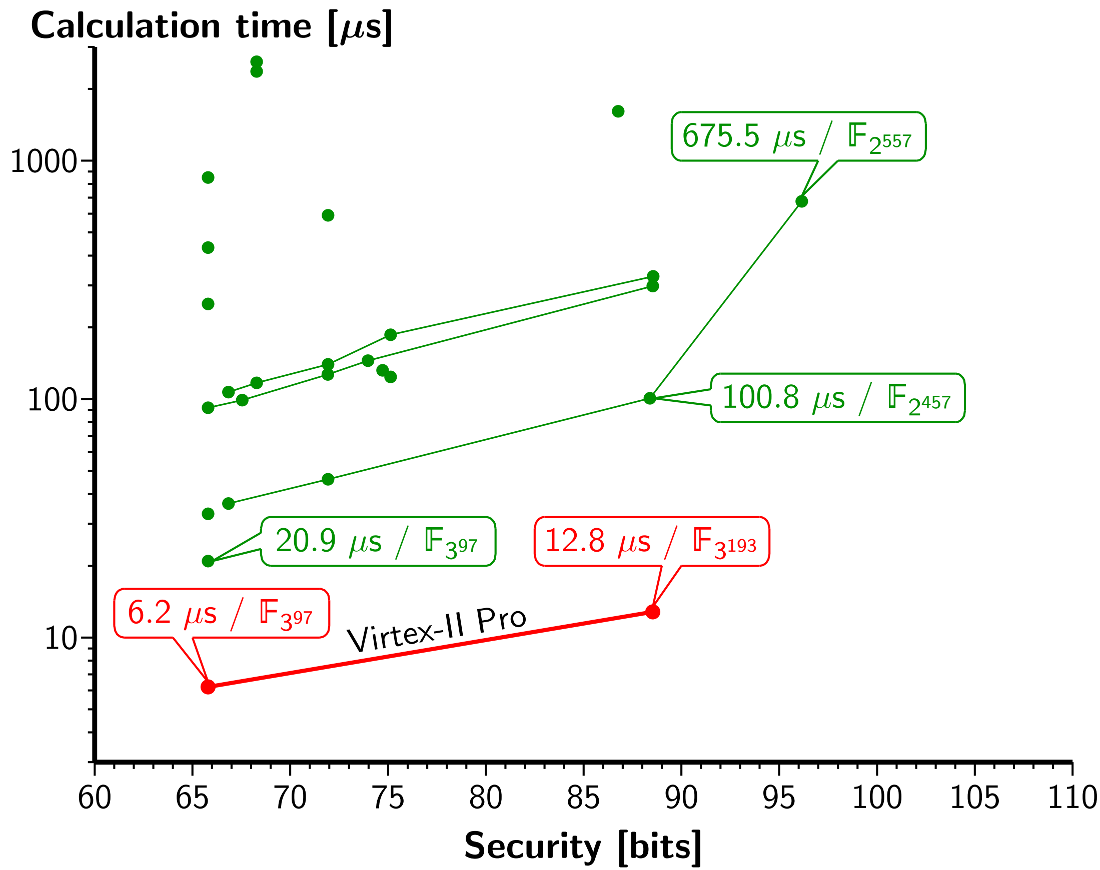
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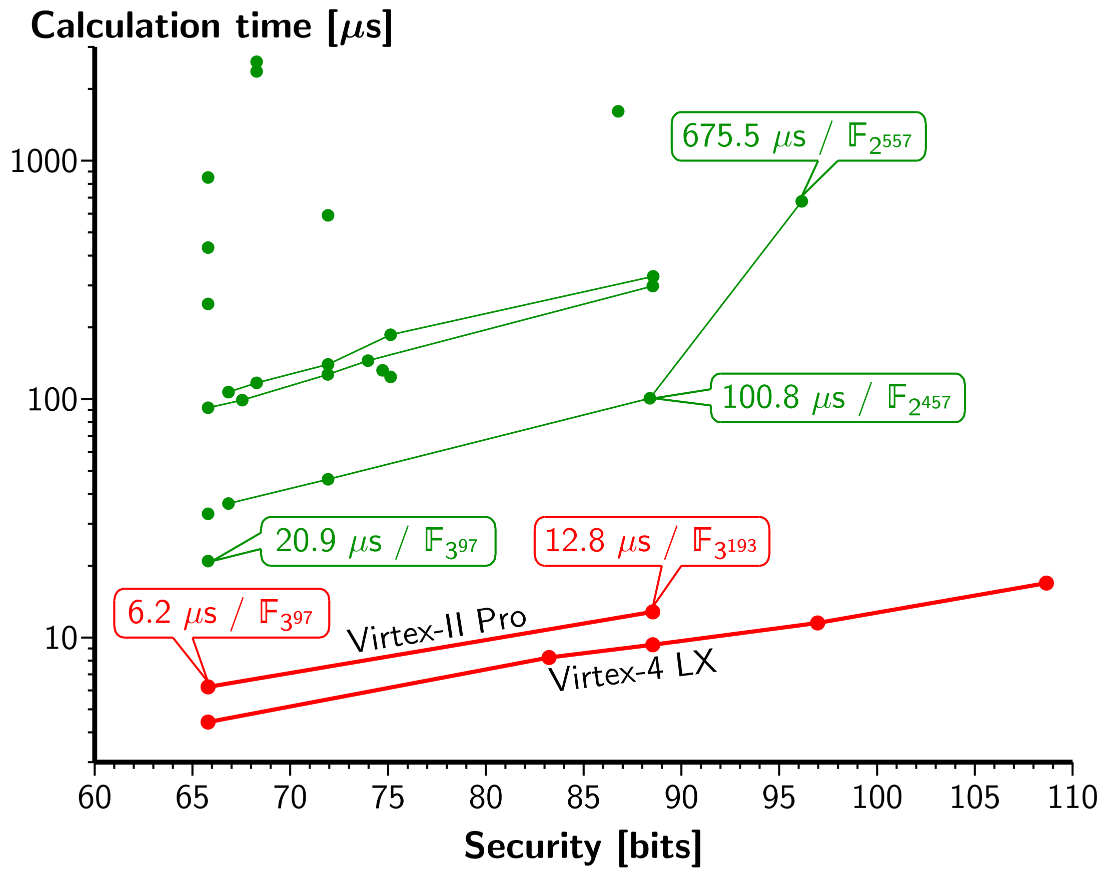
12.8 μs / $\mathbb{F}_{3^{193}}$
6.2 μs / $\mathbb{F}_{3^{97}}$
Virtex-II Pro
60 65 70 75 80 85 90 95 100 105 110
Security [bits]



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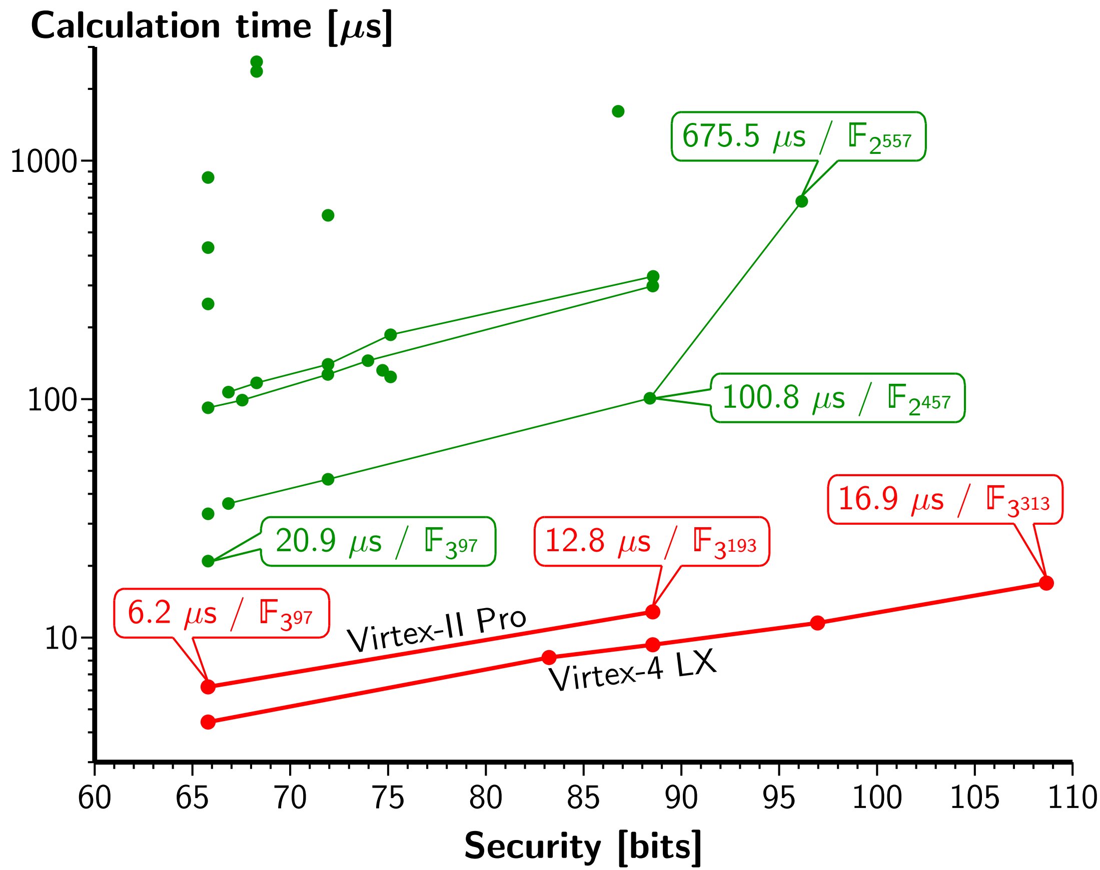
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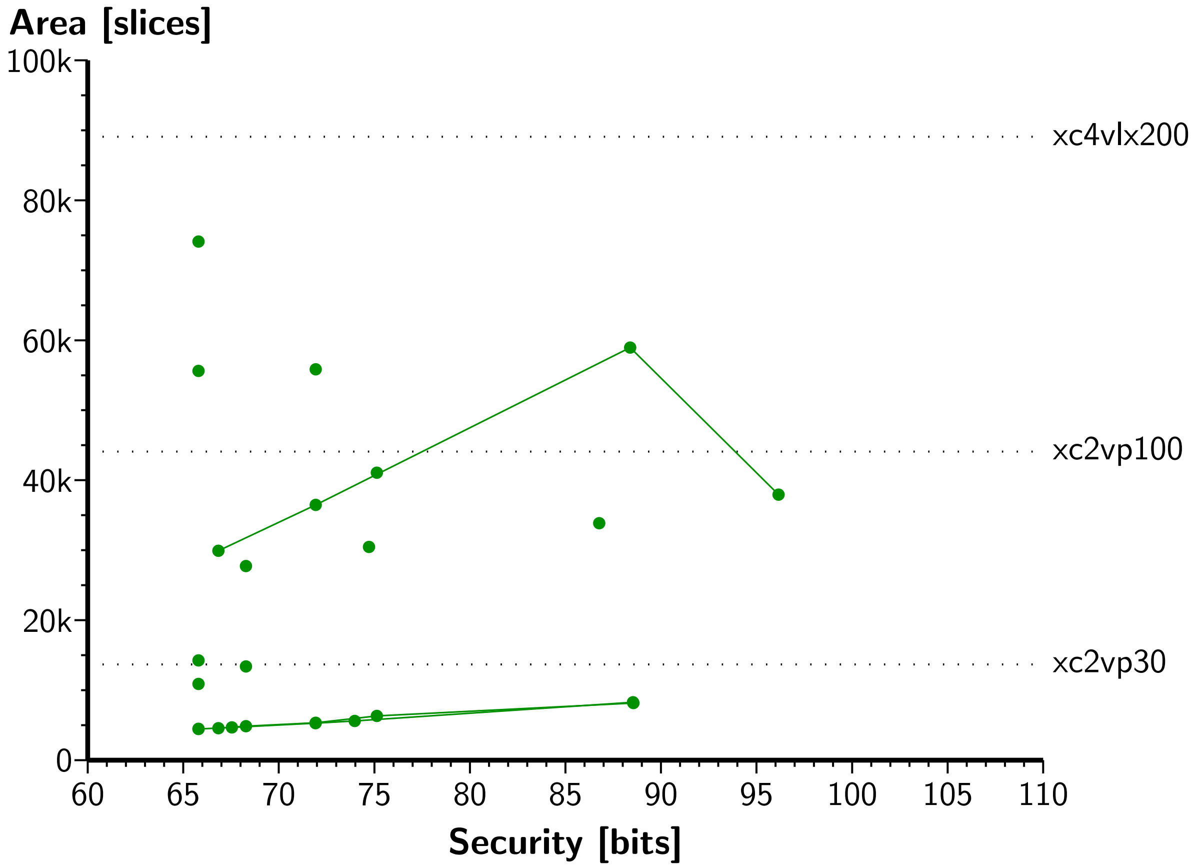
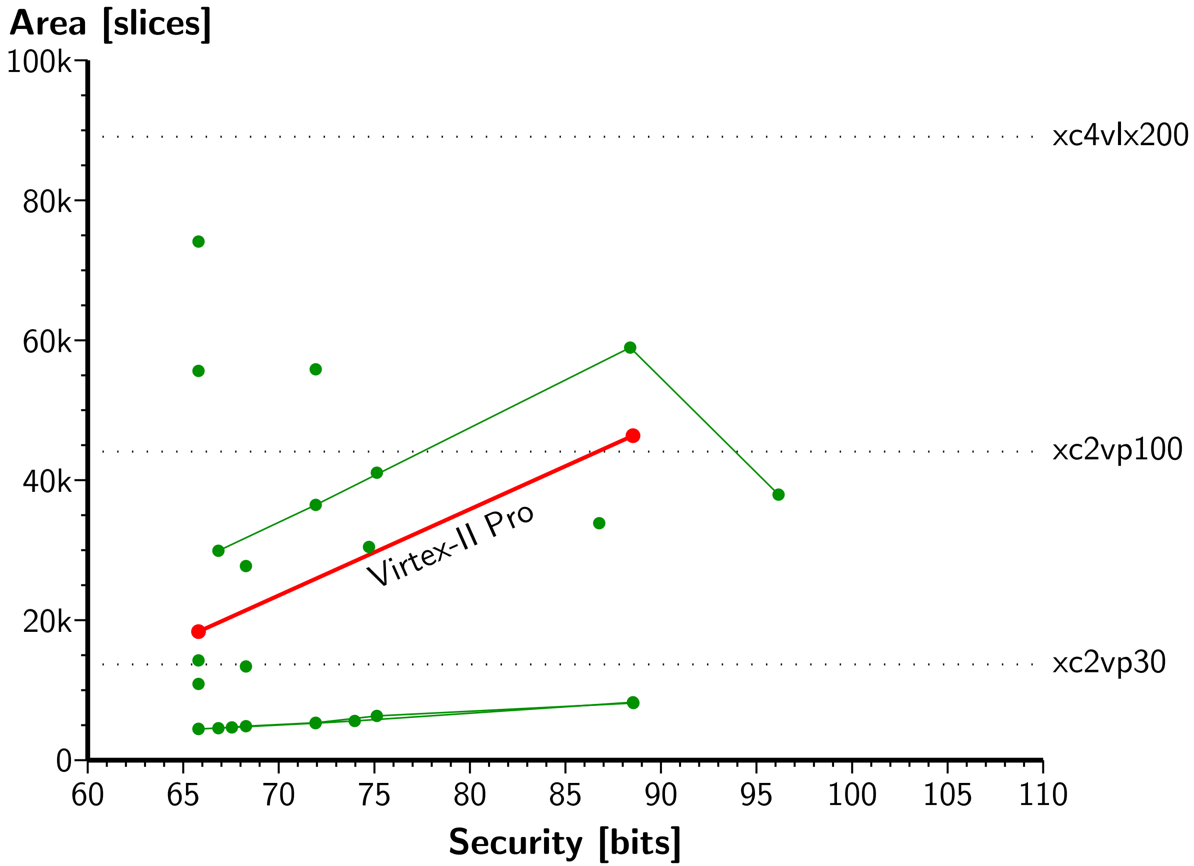
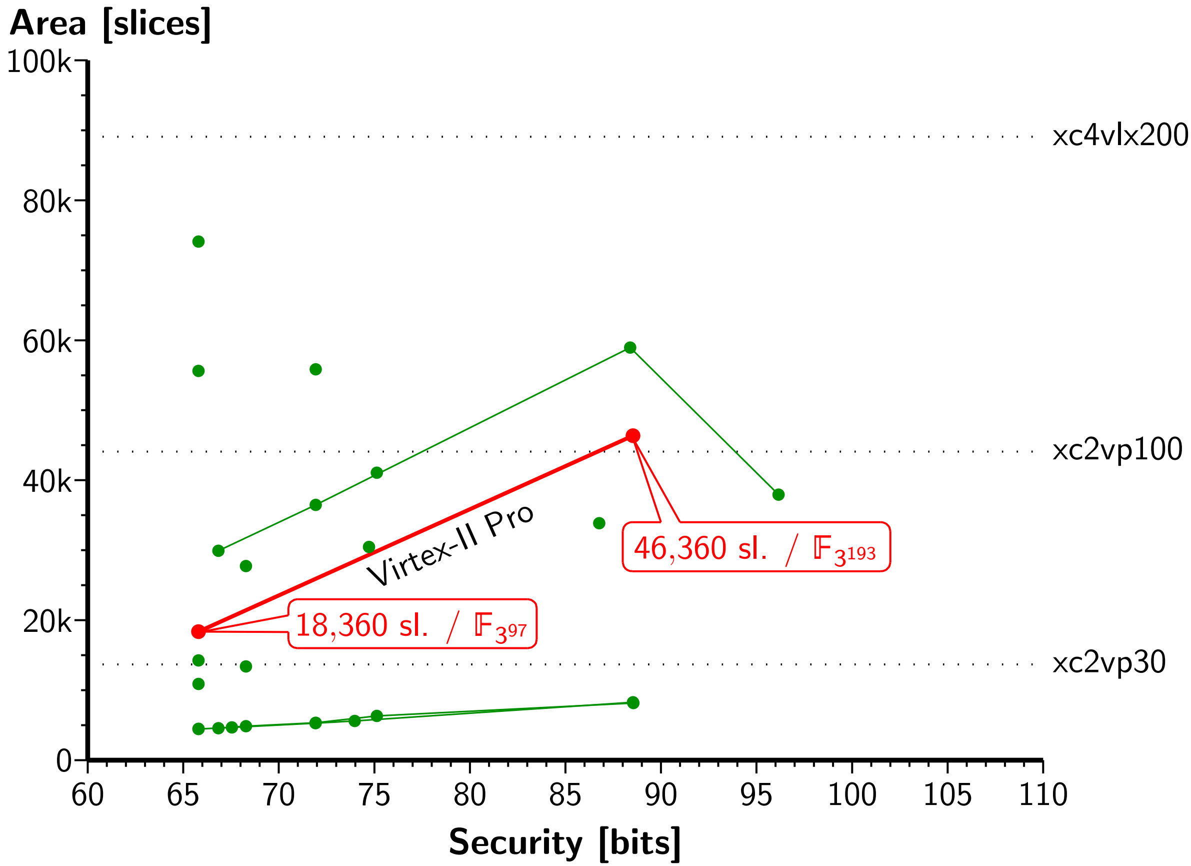
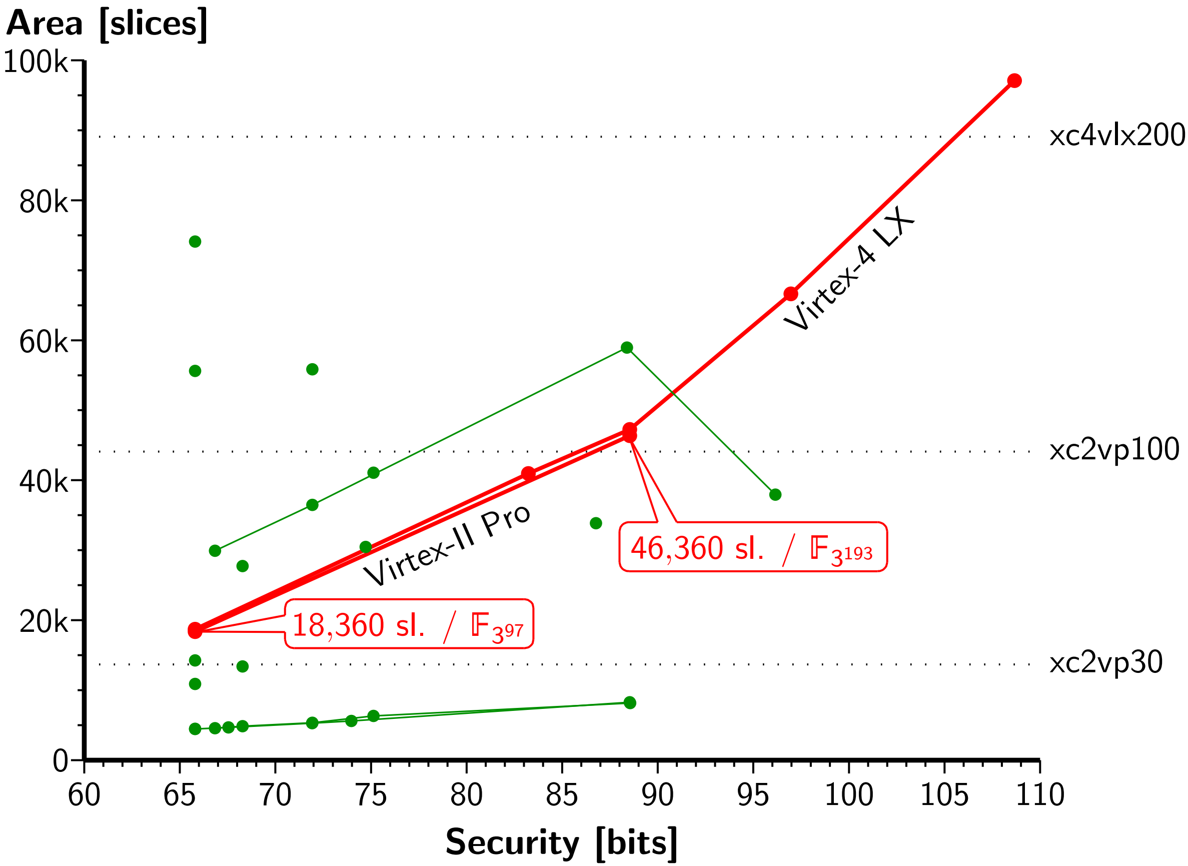
20.9 μs / $\mathbb{F}_{3^{97}}$
16.9 μs / $\mathbb{F}_{3^{313}}$
12.8 μs / $\mathbb{F}_{3^{193}}$
6.2 μs / $\mathbb{F}_{3^{97}}$
Virtex-II Pro
Virtex-4 LX
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

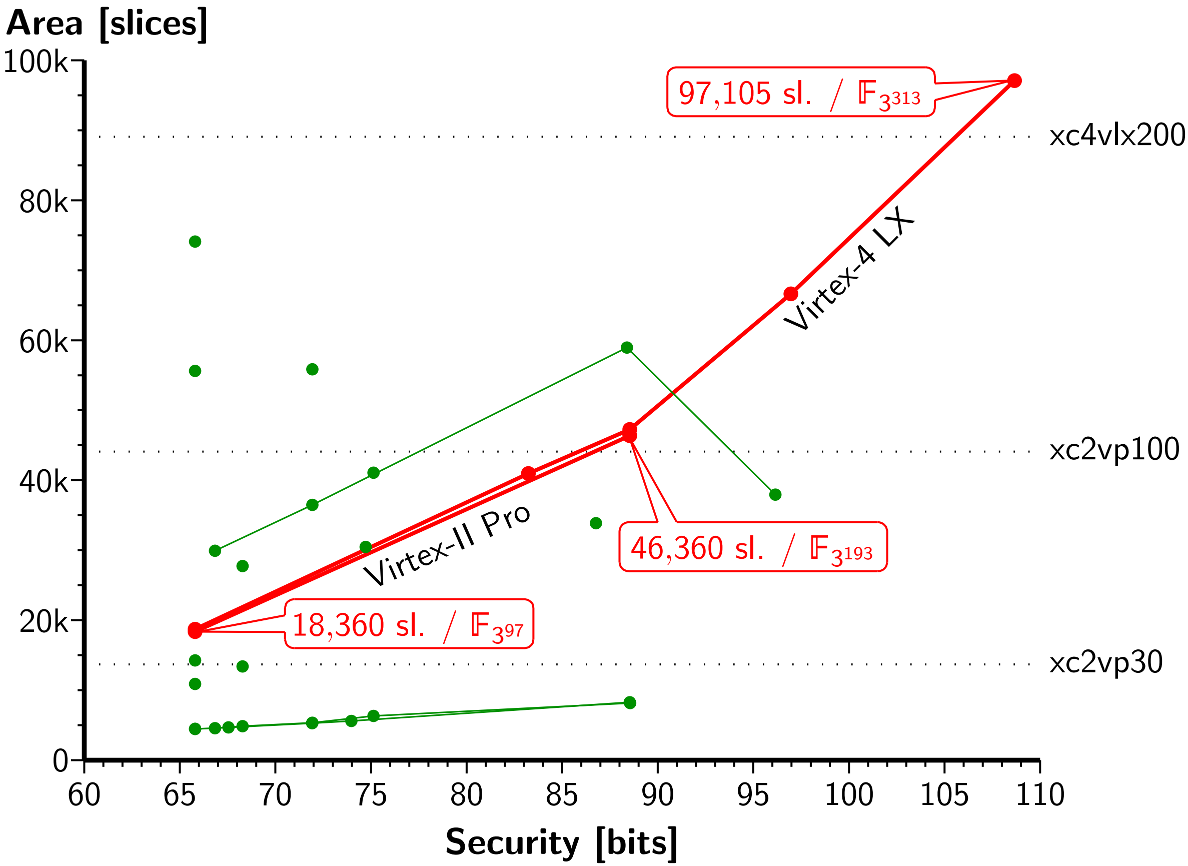

Area [slices]
100k
80k
60k
40k
20k
0
xc4vlx200
xc2vp100
xc2vp30
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

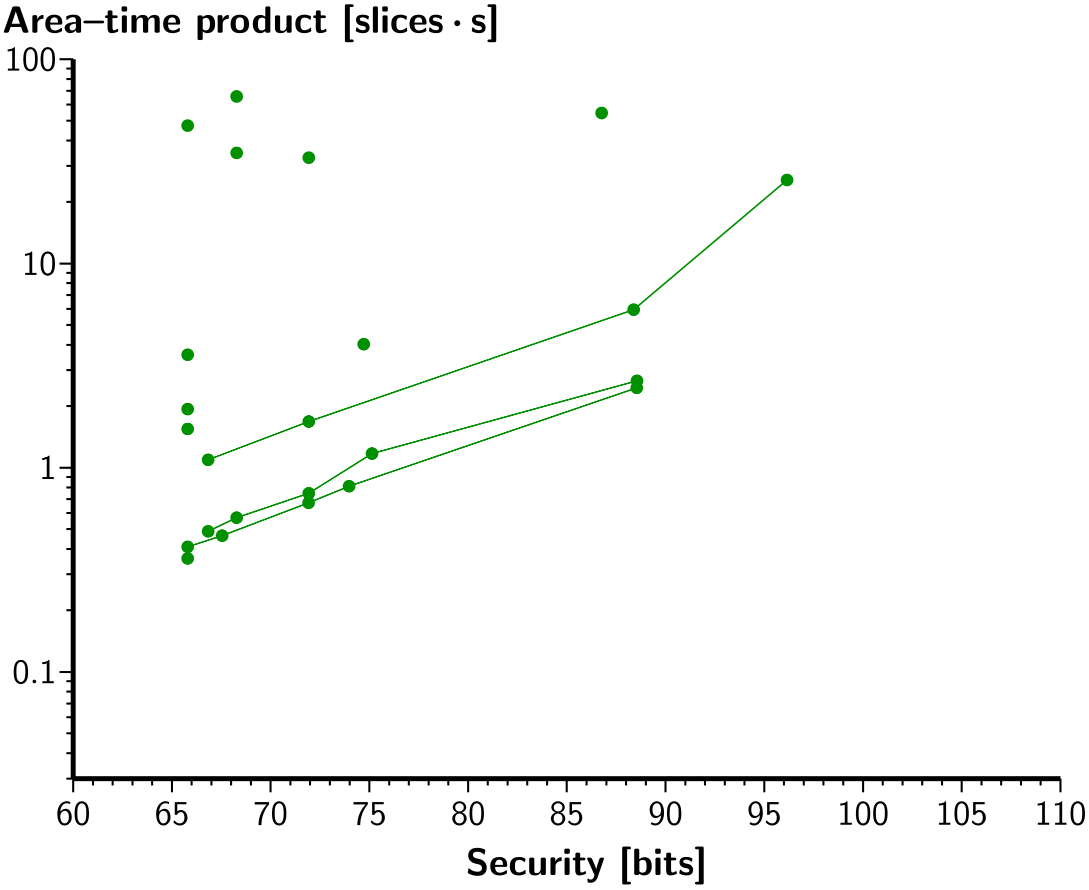

Area [slices]
100k
80k
60k
40k
20k
0
xc4vlx200
xc2vp100
xc2vp30
Virtex-II Pro
60
65
70
75
80
85
90
95
100
105
110
Security [bits]


Area [slices]
100k
80k
60k
40k
20k
0
xc4vlx200
xc2vp100
xc2vp30
Virtex-II Pro
46,360 sl. / $\mathbb{F}_{3^{193}}$
18,360 sl. / $\mathbb{F}_{3^{97}}$
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

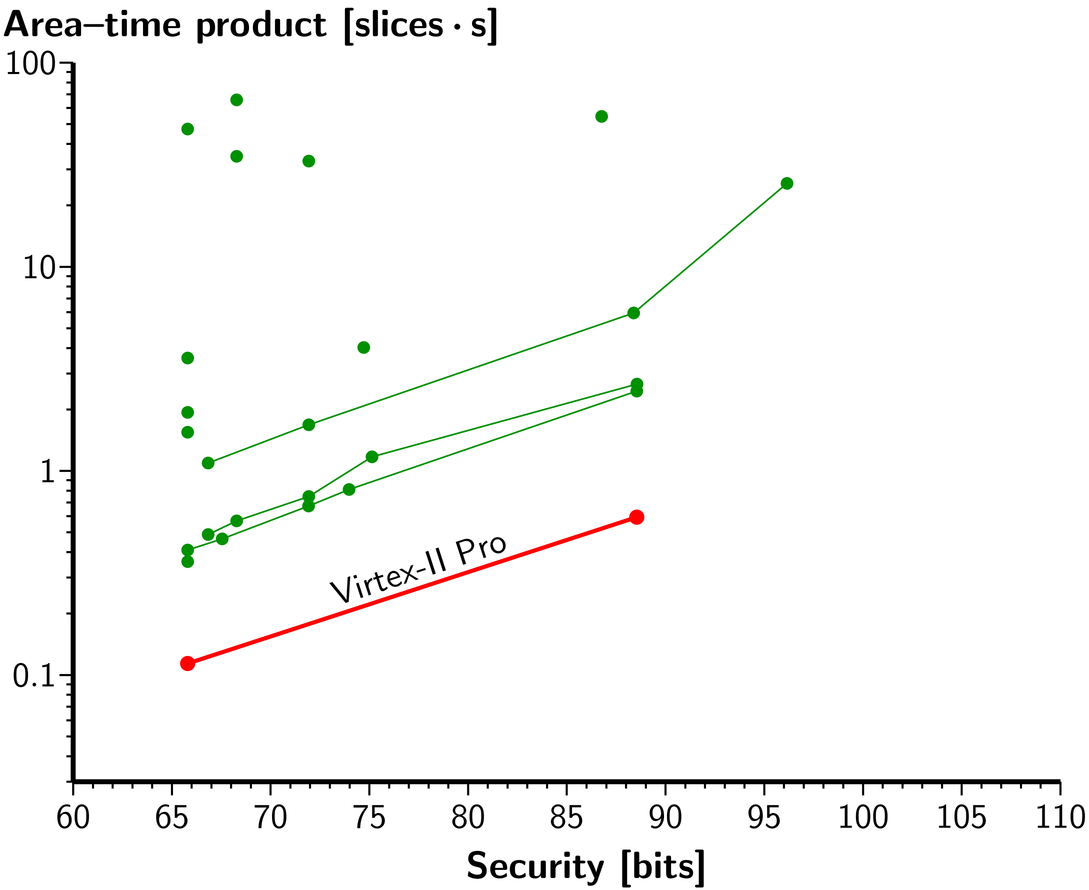


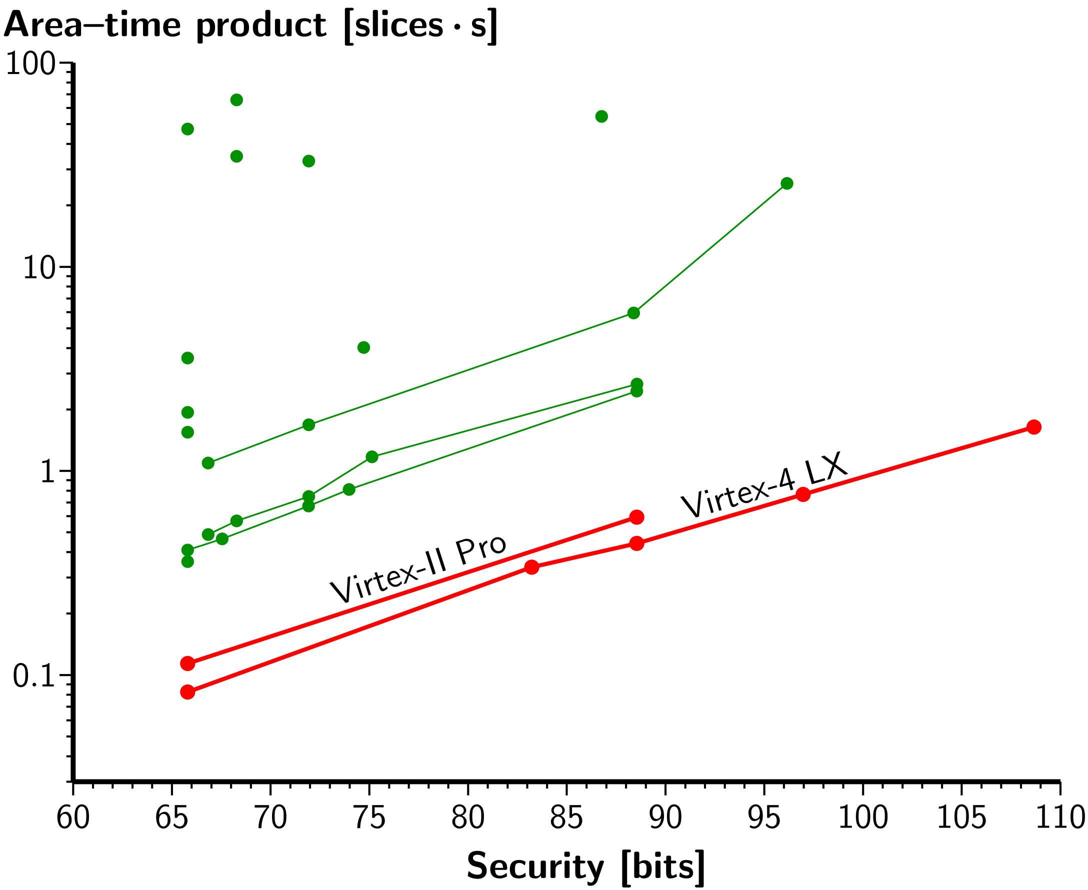
Area [slices]
100k
80k
60k
40k
20k
0
xc4vlx200
xc2vp100
xc2vp30
Virtex-4 LX
Virtex-II Pro
46,360 sl. / $\mathbb{F}_{3^{193}}$
18,360 sl. / $\mathbb{F}_{3^{97}}$
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

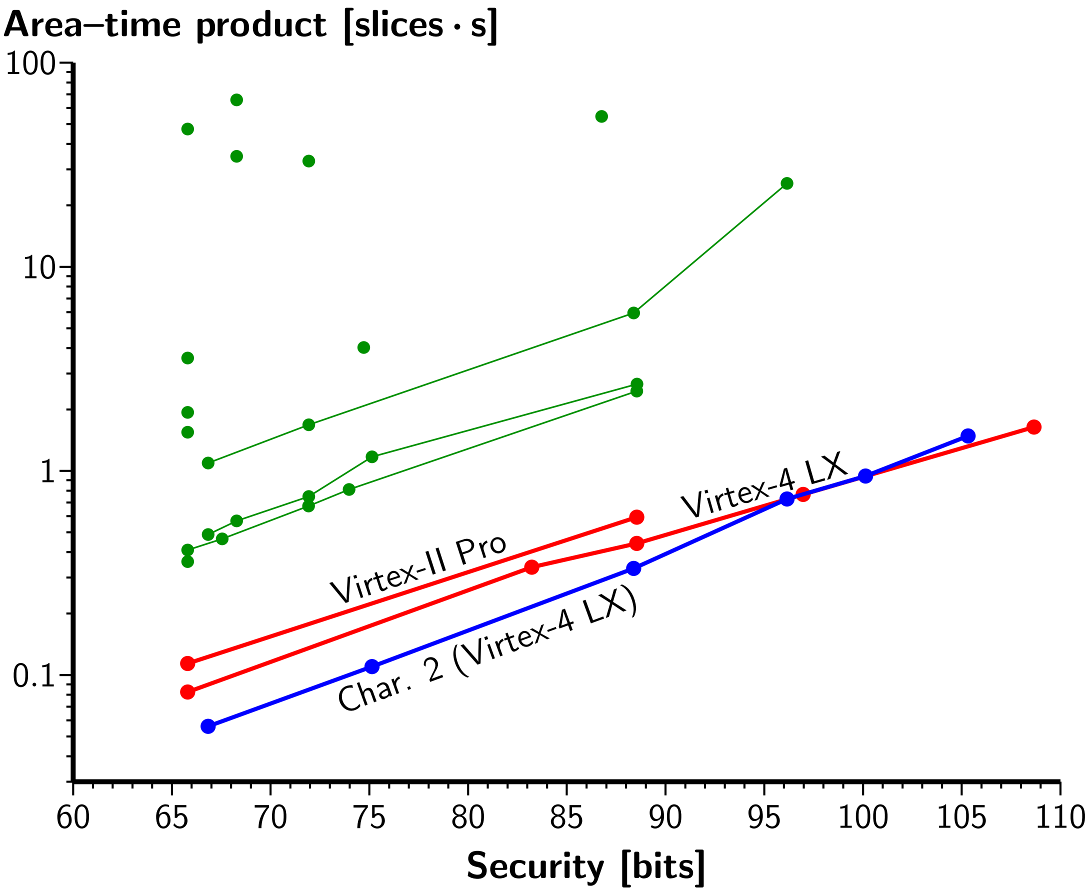

Area [slices]
100k
80k
60k
40k
20k
0
97,105 sl. / $\mathbb{F}_{3^{313}}$
xc4vlx200
Virtex-4 LX
xc2vp100
Virtex-II Pro
46,360 sl. / $\mathbb{F}_{3^{193}}$
18,360 sl. / $\mathbb{F}_{3^{97}}$
xc2vp30
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

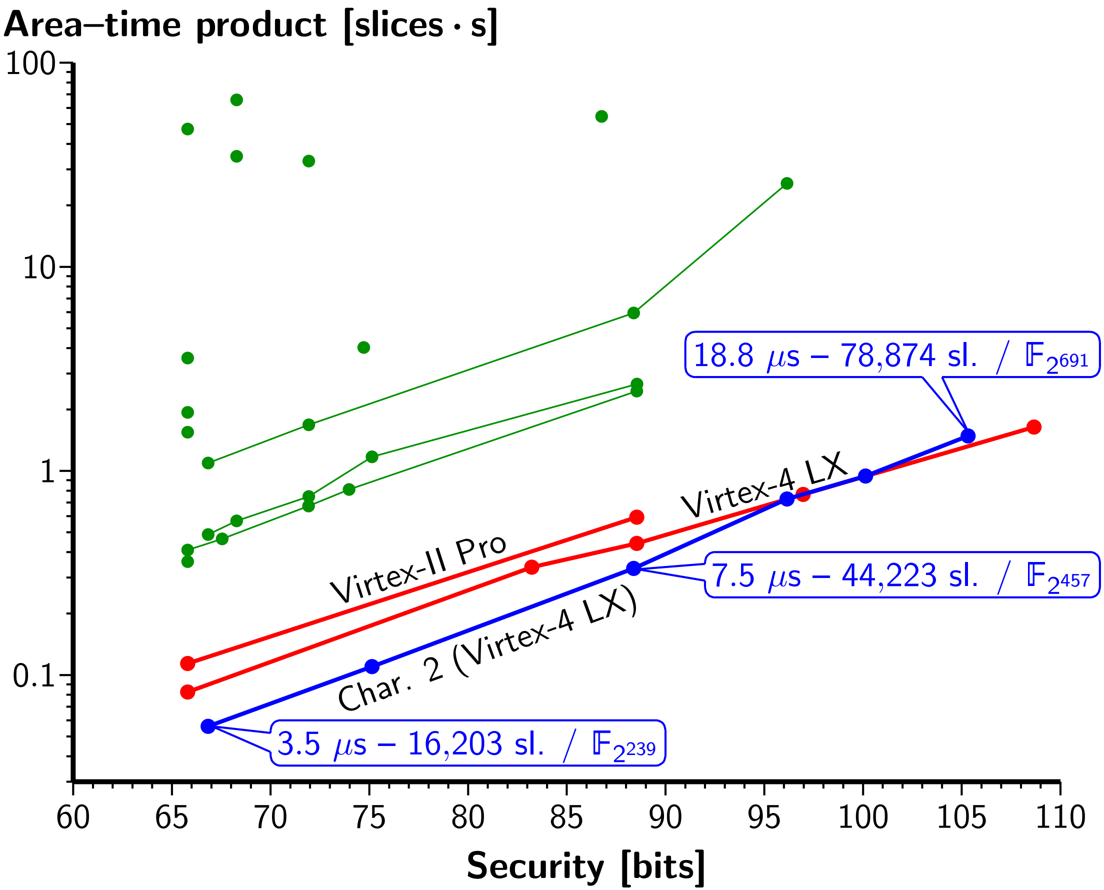


Area–time product [slices · s]
100
10
1
0.1
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

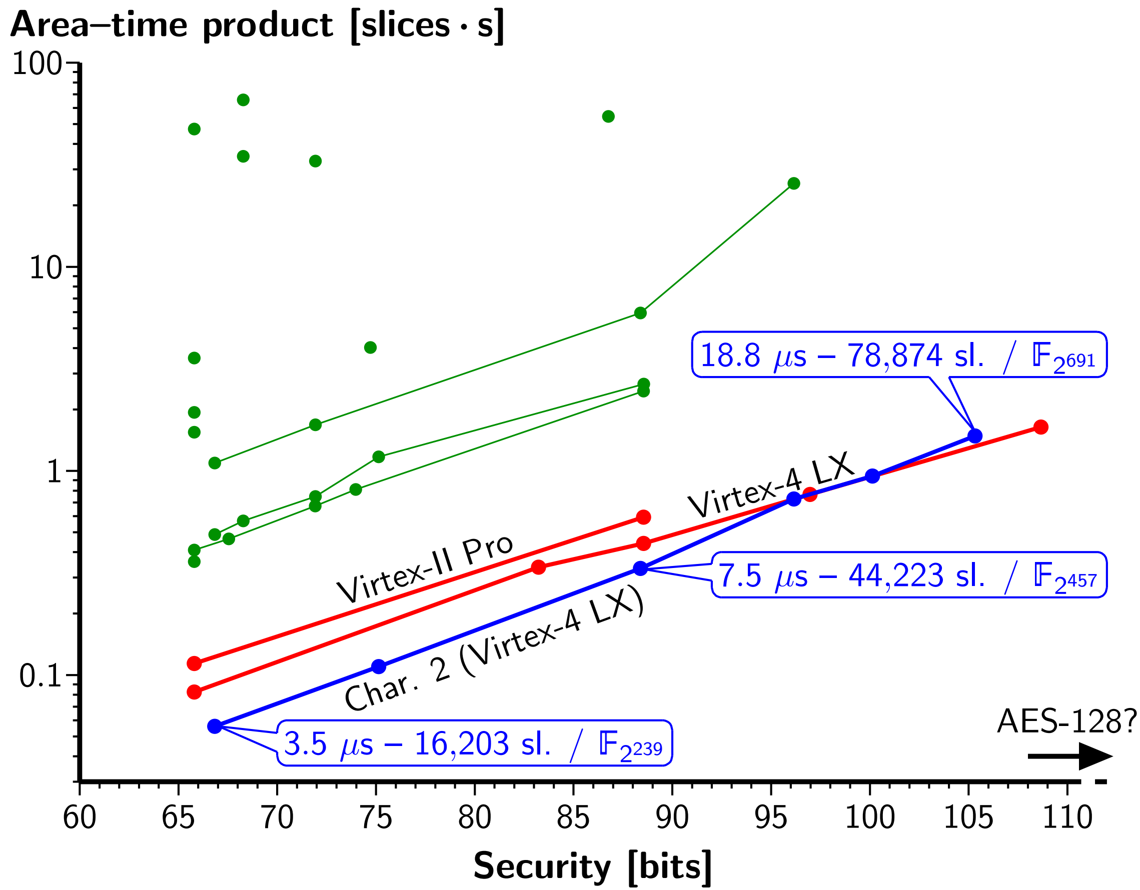

Area–time product [slices · s]
100
10
1
0.1
Virtex-II Pro
60
65
70
75
80
85
90
95
100
105
110
Security [bits]


Area–time product [slices · s]
100
10
1
0.1
Virtex-II Pro
Virtex-4 LX
60
65
70
75
80
85
90
95
100
105
110
Security [bits]


Area–time product [slices · s]
100
10
1
0.1
60
65
70
75
80
85
90
95
100
105
110
Security [bits]
Virtex-II Pro
Virtex-4 LX
Char. 2 (Virtex-4 LX)



Area–time product [slices · s]
100
10
1
0.1
60
65
70
75
80
85
90
95
100
105
110
Security [bits]
18.8 μs – 78,874 sl. / $\mathbb{F}_{2^{691}}$
Virtex-4 LX
Virtex-II Pro
7.5 μs – 44,223 sl. / $\mathbb{F}_{2^{457}}$
Char. 2 (Virtex-4 LX)
3.5 μs – 16,203 sl. / $\mathbb{F}_{2^{239}}$



Area–time product [slices · s]
100
10
1
0.1
18.8 μs – 78,874 sl. / $\mathbb{F}_{2^{691}}$
Virtex-4 LX
Virtex-II Pro
7.5 μs – 44,223 sl. / $\mathbb{F}_{2^{457}}$
Char. 2 (Virtex-4 LX)
AES-128?
3.5 μs – 16,203 sl. / $\mathbb{F}_{2^{239}}$
60
65
70
75
80
85
90
95
100
105
110
Security [bits]

Outline of the talk

- Pairing-based cryptography
- Hardware accelerator for the Tate pairing
- Implementation results
- Concluding thoughts

Conclusion

- A new architecture for pairing computation
  - two specialized coprocessors
  - bet on parallelizing multiplier
  - based on Karatsuba multiplication scheme
  - importance of architecture–algorithm co-design
  - careful bubble-free scheduling of Miller's loop

Conclusion

- A new architecture for pairing computation
  - two specialized coprocessors
  - bet on parallelizing multiplier
  - based on Karatsuba multiplication scheme
  - importance of architecture–algorithm co-design
  - careful bubble-free scheduling of Miller's loop
- High-performance accelerator
  - the fastest coprocessor (17 μs for 109 bits of security)
  - the best area–time trade-off
  - scales to higher security levels

Future work

- Fully parallel multipliers
  - try other algorithms: Toom–Cook, Montgomery's formulae

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  - try other algorithms: Toom–Cook, Montgomery's formulae
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Future work

- Fully parallel multipliers
  - try other algorithms: Toom–Cook, Montgomery's formulae
- Final-exponentiation coprocessor
  - full-featured finite-field processor
  - compute the full pairing with it (work in progress)
- Toward AES-128 security level
  - characteristic 2 (recently submitted)
  - genus-2 supersingular curves in characteristic 2 (work in progress)
  - Barreto–Naehrig curves

Thank you for your attention

Questions?