Title.
Graph neural networks for on-chip communication interconnect design

Context and motivation.
High-performance embedded computing systems heavily rely on on-chip communication interconnects to meet their performance requirements. Several thousands of cores can be connected via such interconnects to exchange data. Therefore, communication interconnects must be designed in an efficient manner. In general, it is very challenging to explore the design space of these interconnects, which are usually described as graphs.
To address this issue, a recent study investigated a generative artificial intelligence method [1]. They use an arbitrary graph representation to capture the interconnections. Then, by using trained generative adversarial networks, relevant interconnect graphs can be automatically generated. Results from this preliminary study are promising.

Goal of the project.
As part of this internship, we would like to investigate the impact of various graph representations [2] [3] on the prediction accuracy of artificial neural networks. Another potential issue of interest concerns the scalability of the target interconnects, beyond those used in [1]. So, the most favorable graph representations should be able to suitably address the potential scalability limitation of graph-related neural network training.

The successful applicant to this project is expected to have some knowledge of graph theory, and be open to applying AI or data science methods.

Keywords.
Graph representation, graph generation, graph neural networks, spectral versus spatial representation

Contact information.
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LIRMM is a cross-faculty research entity of the University of Montpellier and the National Center for Scientific Research (CNRS). Located in Montpellier, LIRMM is one of the largest multi-disciplinary research laboratories in Europe. Its Microelectronics department carries out cutting-edge research in the fields of design and testing integrated systems and micro-systems, with a focus on architectural aspects, modeling and methodology.

References.
[1] Maxime Mirka, Maxime France-Pillois, Gilles Sassatelli, Abdoulaye Gamatié. “A Generative AI for Heterogeneous Network-on-Chip Design Space Pruning” DATE 2022: 1135-1138

[2] http://users.cecs.anu.edu.au/~bdm/nauty/

[3] Muhammet Balcilar, Guillaume Renton, Pierre Héroux, Benoît Gaüzère, Sébastien Adam, et al.. “Bridging the Gap Between Spectral and Spatial Domains in Graph Neural Networks”. 2020. ⟨hal-02515637⟩