Interference analysis for the new Kalray MPPA3 many-core

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1 Context

In automotive and avionics, some programs are subject to critical timing constraints. In these real-time critical systems, the timing properties must be guaranteed. Among them, the worst-case execution time that guarantees an upper-bound on the execution time of programs. On a multi-core platform, this worst-case execution is highly influenced by all concurrent programs. In our work, we studied the Kalray MPPA2 platform (a set of multi-core communicating through a network on chip comprising 256 compute cores, designed by a company located in Montbonnot, near Grenoble), and designed an algorithm able to tightly bound the interference. Our interference analysis models the interference on the memory bus and the communications through the network-on-chip.

2 Internship proposal

This analysis showed very good results in terms of precision, but is limited in terms of scalability (the overall algorithm is O(nˆ4) in number of tasks). We already have ideas on how to reduce the complexity and improve the scalability (by changing the way we iterate to find a solution), and on how to improve the precision further (through a better study of the communication, memory accesses and scheduling). The aim of this internship is to explore one of the improvement axis and implement it in our analysis tool.

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