Scalability of the interference analysis for a multi-core platform

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1 Context

In automotive and avionics, some programs are subject to critical timing constraints. In these real-time critical systems, the timing properties must be guaranteed. Among them, the worst-case execution time that guarantees an upper-bound on the execution time of programs. On a multi-core platform, this worst-case execution is highly influenced by all concurrent programs. In our work, we studied the Kalray MPPA2 platform (a set of multi-core communicating through a network on chip comprising 256 compute cores, designed by a company located in Montbonnot, near Grenoble), and designed an algorithm able to tightly bound the interference, taking into account both the specificities of the software application and the low-level details of the hardware architecture. Our interference analysis models the interference on the memory bus and the communications through the network-on-chip.

2 Internship proposal

In the new generation of chip, the MPPA3 (announced in 2017), considerable changes have been made to the architecture (less clusters but faster communications and memory access). The generic part of our algorithm are still valid, but the mathematical model of the hardware architecture must be redesigned. The goal of the internship is to analyze how far our previous work may be adapted to this new platform and propose modified/new interference analysis.

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