CASH
Compilation and Analysis, Software and Hardware
Optimization and Dataflow Parallelism for HPC Applications

Compiling and Scheduling Dataflow Programs

- Objectives:
  - Unify all kinds of parallelism in a single semantic framework (intermediate representation)
  - Validation on literature examples (video algorithms, neural networks)
  - Implement a mature compiler infrastructure/toolbox

Scalable Static Analyses

- Objectives:
  - Revisit syntax-based optimizations and polyhedral model in the AI framework
  - Design new low cost analyses
  - Find a theoretical framework to design scalable analyses
  - Better interfaces for analyses and their optimization clients

Hardware Compilation for FPGA and Dataflow Optimization

- Objectives:
  - Cost models for FPGA and fast simulation algorithms
  - Optimization of data transfers, throughput, and circuit surface
  - Hierarchical dataflow models for scaling synthesis
  - Synthesis of hardware with dynamic control/data

Simulation of Hardware

- Objectives:
  - Heterogeneous simulation (functional + multi-physics, precise/abstract)
  - Scale up (~ parallelism)

Industrial collaborations:
- Kalray (Many-Core), STMicroelectronics, XtremeLogic (Inria spin-off).
- Approach: cross-fertilization between complementary domains
  - High-level synthesis (HLS) + high-performance compilation
  - Diverse formal reasoning methods
  - Compilation + abstract interpretation

CASH Members:
- Christophe Alias (CR, Inria)
- Julien Braine (Ph.D student)
- Laure Gonnot (MCF, Univ. Lyon1)
- Ludovic Henrio (CR, CNRS)
- Paul Iannetta (Ph.D student)
- Laetitia Lecot (Inria assistant)
- Matthieu Moy (Team Leader, MCF, Univ. Lyon1)

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