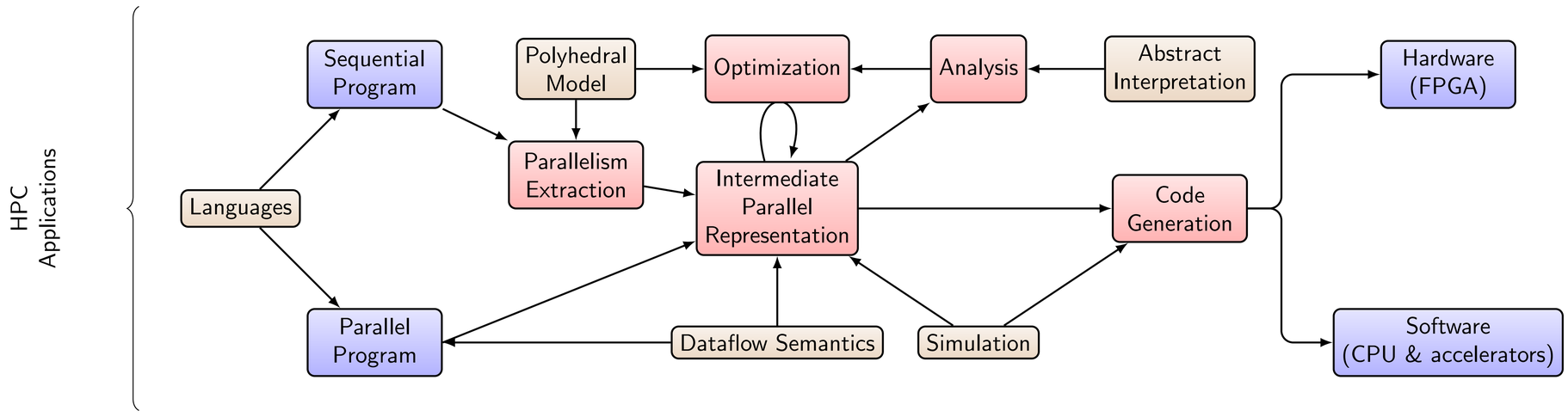
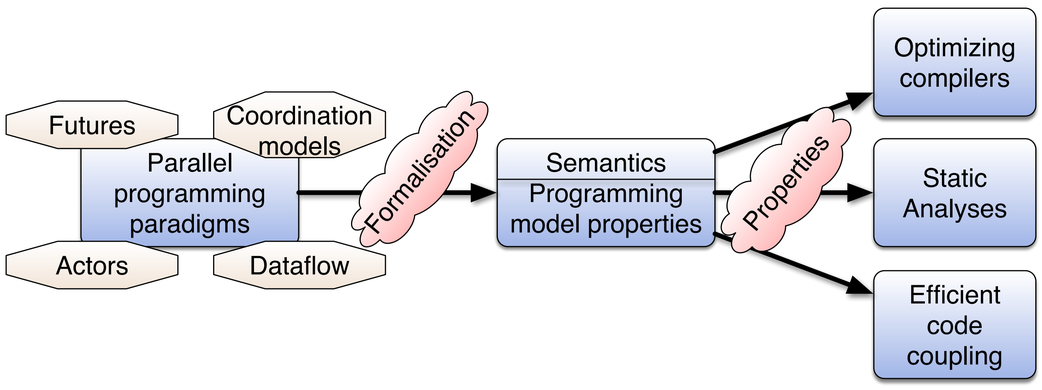
CASH

Compilation and Analysis, Software and Hardware



Parallel & Dataflow Programming Models



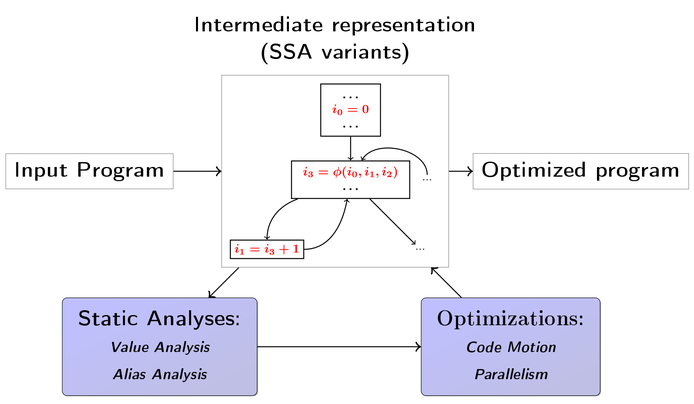
Locks:

- Different granularity levels
- Different paradigms (shared/distributed memory, message passing)

Objectives:

- Study semantics and combinations of paradigms
- Validate on literature examples (video algorithms, neural networks, ...)
- Contribute to mature compiler infrastructures/toolboxes

Scalable Static Analyses



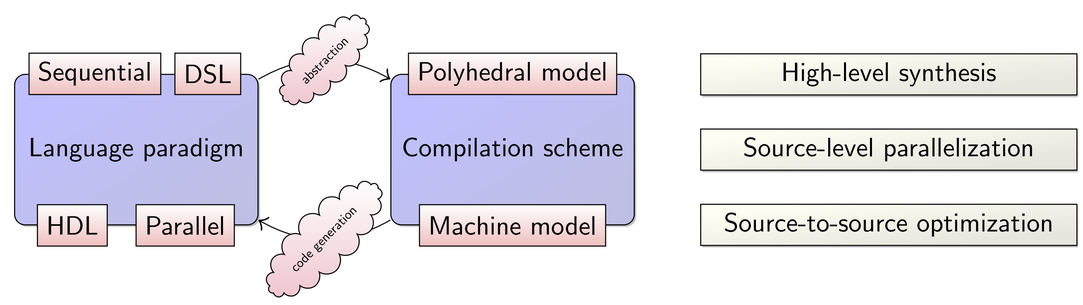
Locks:

- Classic abstract interpretation (AI) too costly
- How to design optimization-oriented analyses?
- Many syntax-based optimizations inside compilers

Objectives:

- Revisit syntax-based optimizations and polyhedral model in the AI framework
- Design new low cost analyses on new optimized IRs.
- Better interfaces for analyses and their optimization clients.
- Understand the link with parallel IRs

HPC Compilation and High-Level Synthesis



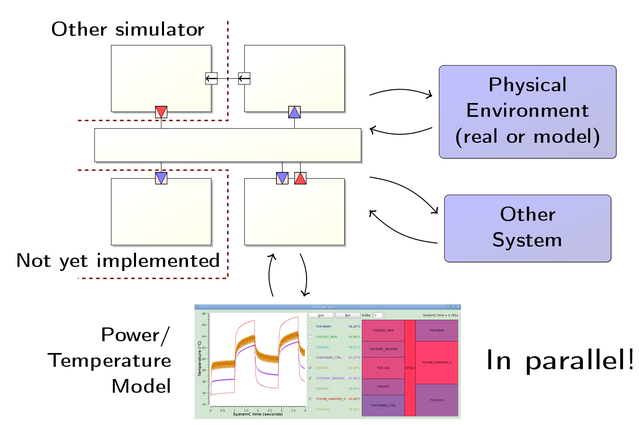
Locks:

- Different levels of parallelism and memory (vector, core, cluster, ...)
- Circuit synthesis bounded by commercial HLS tools

Objectives:

- Develop source-level optimizations for high-level synthesis
- Rephrase the polyhedral model with dataflow semantics
- Contribute to mature compiler infrastructures ⇝ XtremLogic (Inria spin-off)

Simulation of Hardware



Locks:

- Heterogeneous simulation (functional + multi-physics, precise/abstract)
- Scale up (⇝ parallelism)

Objectives:

- Application to simulation of data-aware process networks
- Parallel full-stack (OS + application) simulation
- Simulation of HPC applications on supercomputers

Industrial collaborations

Bull/Atos (HPC), Kalray (Many-Core), STMicroelectronics, XtremLogic (Inria spin-off).

Approach: cross-fertilization between complementary domains

- High-level synthesis (HLS) + high-performance compilation
- Diverse formal reasoning methods / Semantics
- Compilation + abstract interpretation

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