"Power Dissipation Challenges in Optical Transport Systems and Proposed Solutions"

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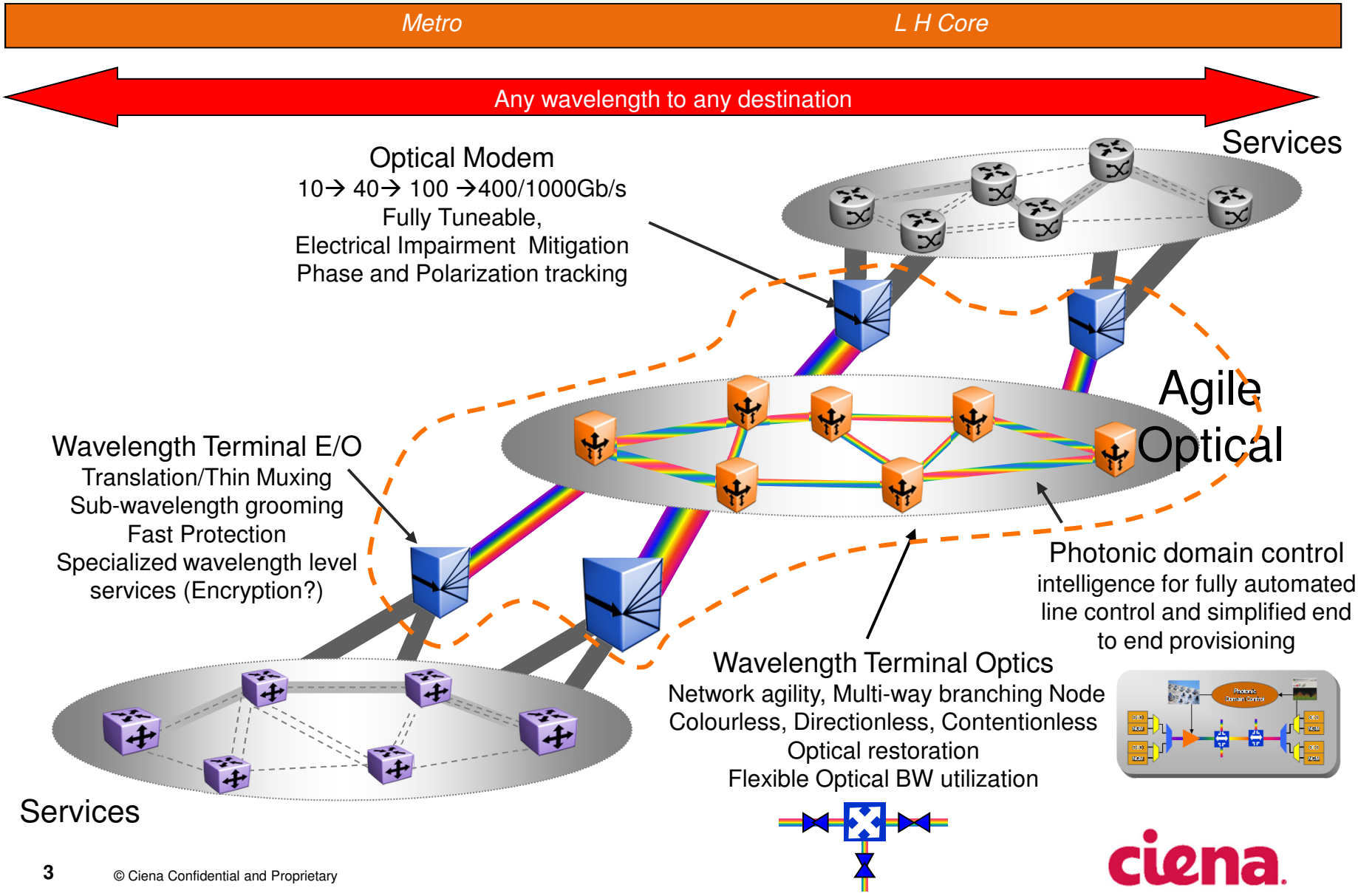
Abstract

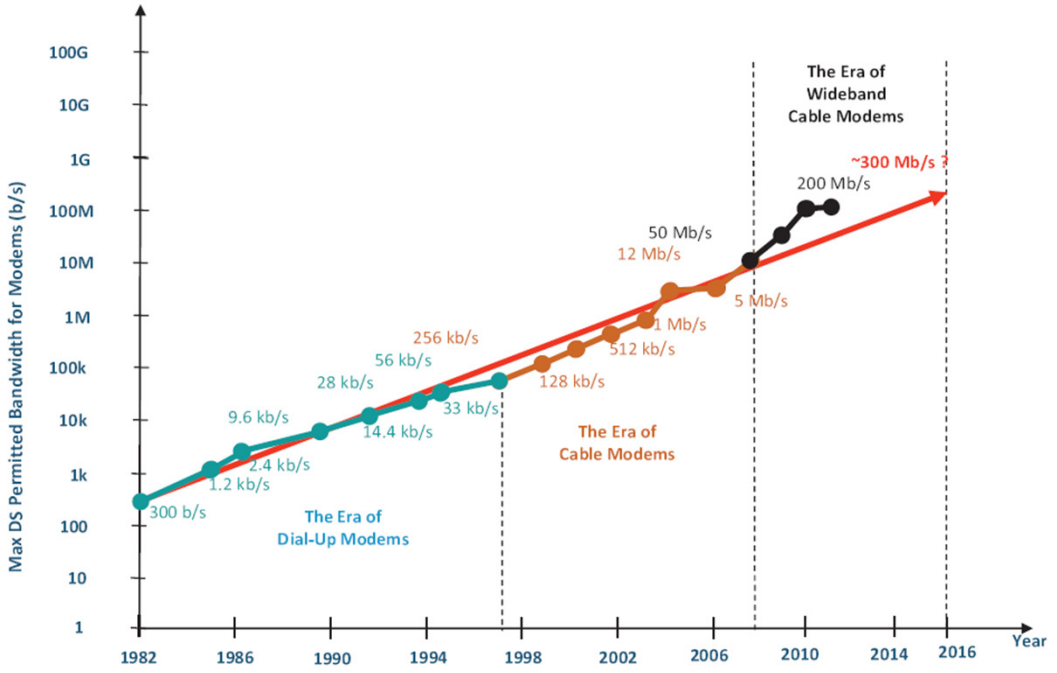
- **Power dissipation on transport optical systems has been a growing problem.**
- **This presentation will suggest a method for improving technology selection and overall power distribution in order to increase the efficiency of the transport system.**
- **A procedure will be suggested for specific integrated circuit, where most of the power dissipation occurs in Transport sub-system.**
- **This procedure will also explain the potential optimization of power sources for an optical system applications.**

Transport in the Network



Bandwidth demands still growing

- **Access demand keep increasing**
- **Constant pressure to transport bits in an efficient method**

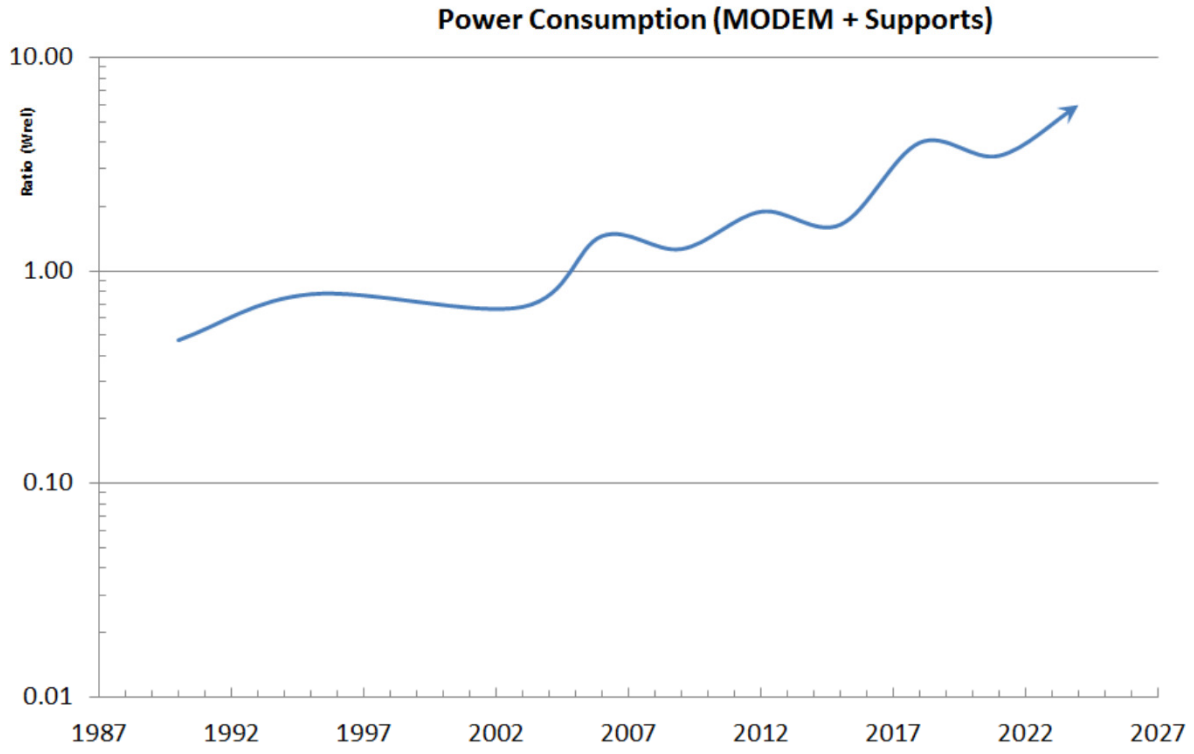


Source: http://www.ieee802.org/3/ad_hoc/bwa/public/sep11/cloonan_01a_0911.pdf

IEEE 802.3 Industry Connections Ethernet Bandwidth Assessment Ad Hoc
July 2012 IEEE 802 Plenary, San Diego, CA, USA

Rear view mirror and full steam ahead; Here lies the pain point!

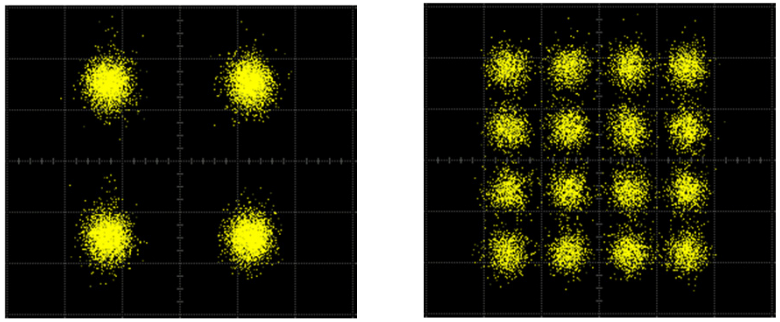
- Power Consumption keep increasing from generation to the next;
- Larger the bandwidth requirements, higher the transistor count, longer wires requires.



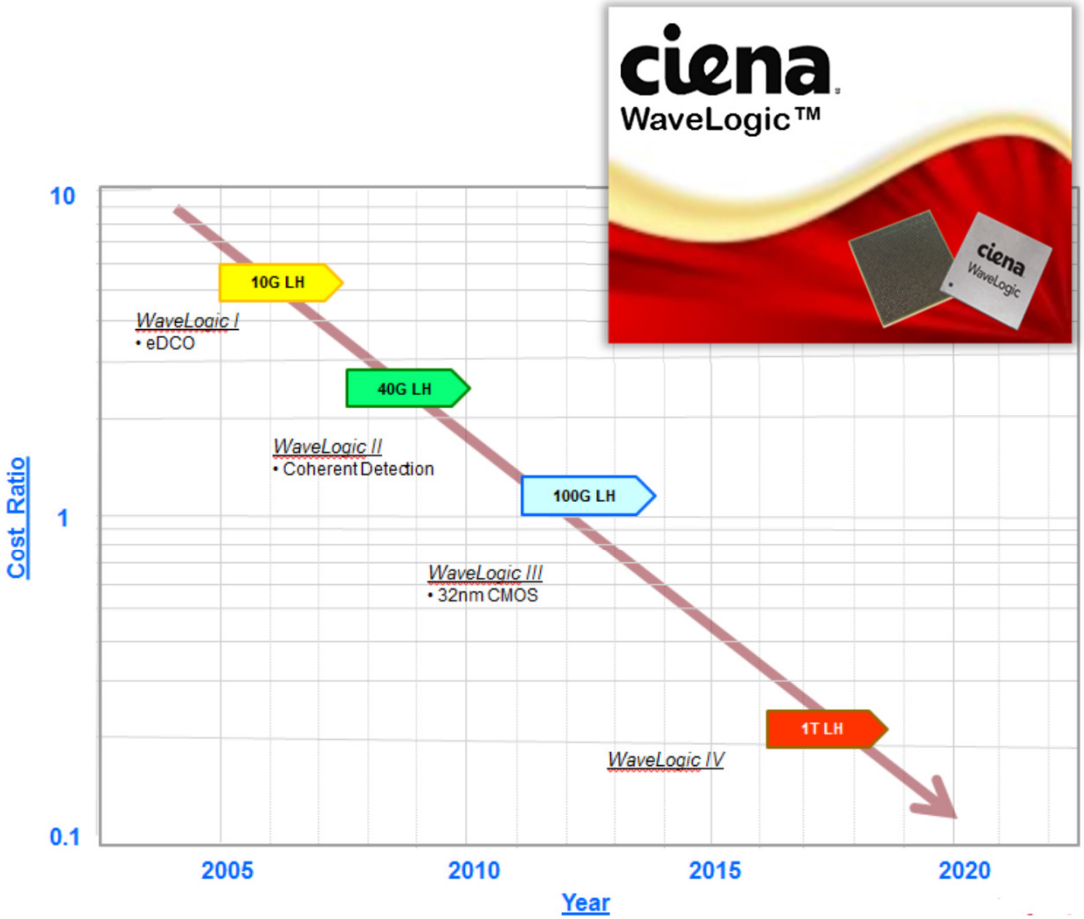
MODEM Cost/bit Trends

- **Customer expect less cost per transport bit for equivalent functionality**
  - Increase Spectral Efficiency

QPSK **16-QAM**

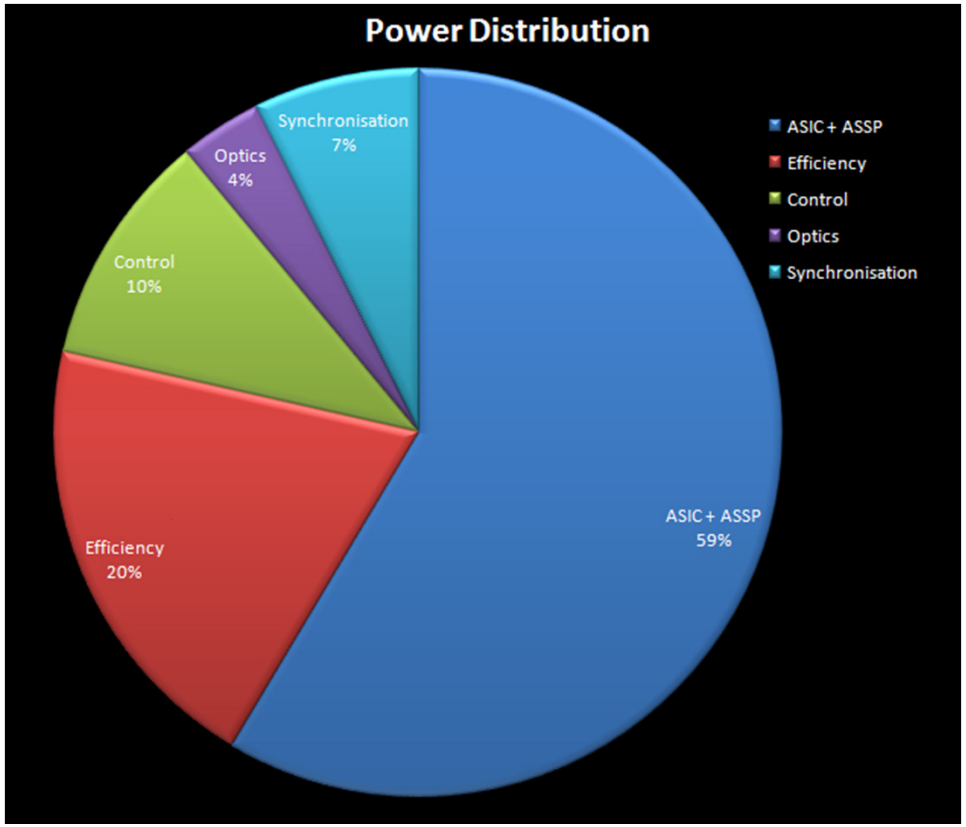


- **Expected trends to continue.**



Typical MODEM Power segmentations

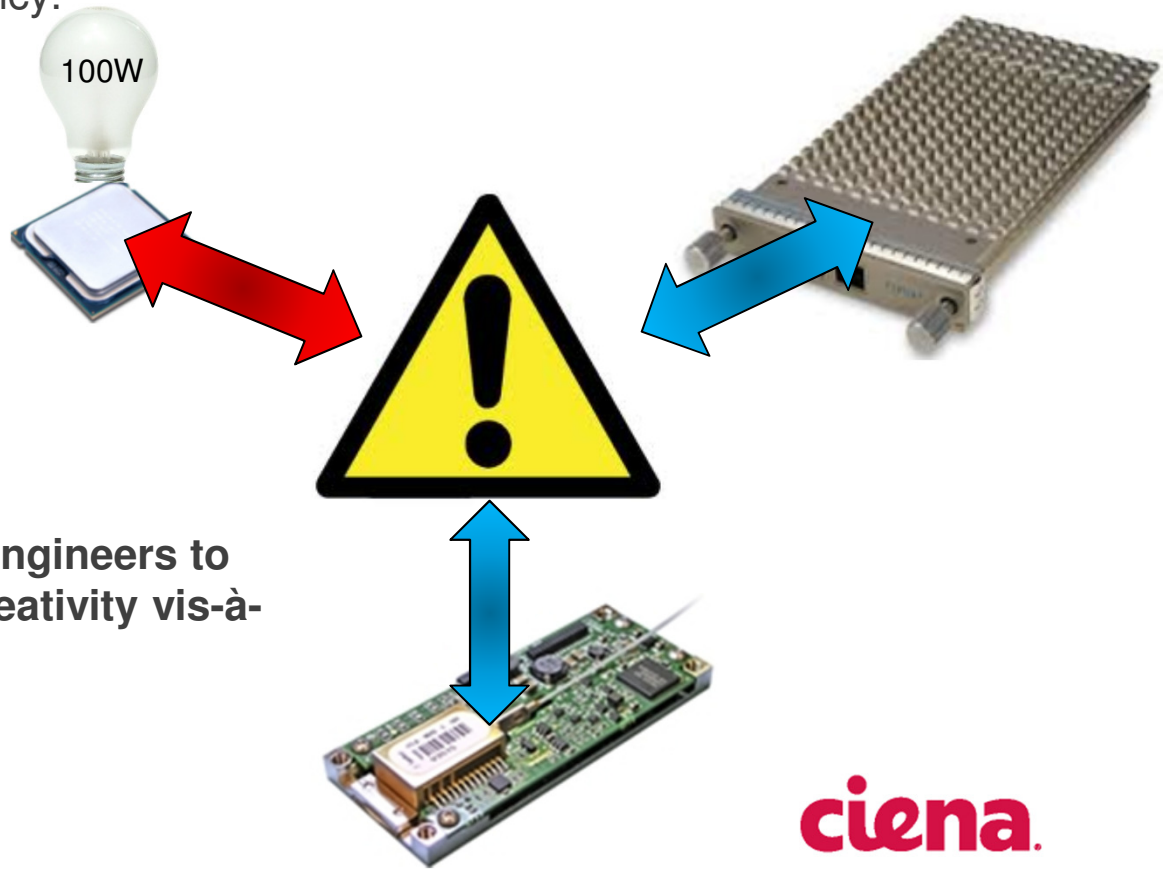
- About 80% of the power consumption comes from various silicon devices such ASPP, ASIC and power conversion inefficiencies.



MODEM/Transponder Co-Location Challenges

- **ASIC "Hot Spots" and Optical devices creates a very challenging environment and require a serious analysis**

  Larger blade footprint to distribute the thermal load and Hot Spots and increase the power delivery efficiency.

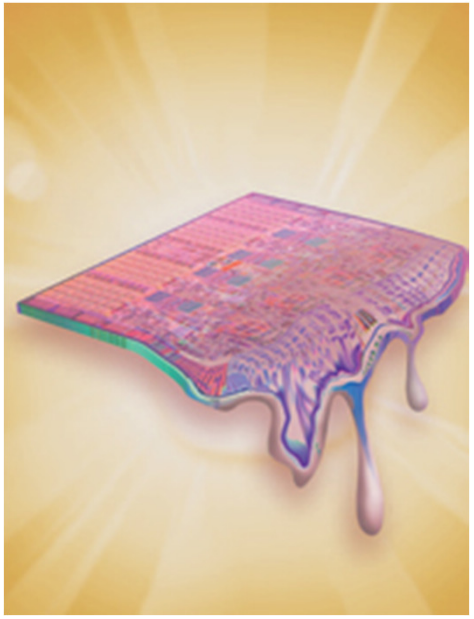


- **The bright side is it forces engineers to create an environment of creativity vis-à-vis overall efficiency**

Big D, Small A Trends

Analog IP is a key part of the Telecom Coherent MODEM development, but not the Power bottleneck;

- Analog power trends from 90nm to 32nm generally flat
- Digital is more than 75% of the total power consumption of today's ASIC for LH and ULH applications.
- Towards 50% for Metro and Regional, applications.



Technology Choices – ASIC, ASSP and Efficiency

- **Applied Semiconductor Integrated Circuit, ASIC, and Applied Specific Standard Product, ASSP, are required for selected IP which couldn't be done efficiently otherwise in our industry.**
- **The partner and process selection is very important and required for every design including;**
  - Intellectual Property, IP, transfer
  - Accurate power dissipation estimations
    - Technology selection
    - CAD Tool selection based on accuracy
      - Less than 20% errors today; towards 10% at the RTL vcd level
  - Standard and Custom model library selection
  - SERDES Performances and power dissipation
    - 2.5Gb/s to 10Gb/s today,
    - Towards 25Gb/s and 40/50Gb/s tomorrow

CMOS Power and Moore's Law

Dynamic:

$P_{dyn} : X^* C_{load}^* V_{dd}^2 * Tr$

Tr = Toggle rate

Short Circuit

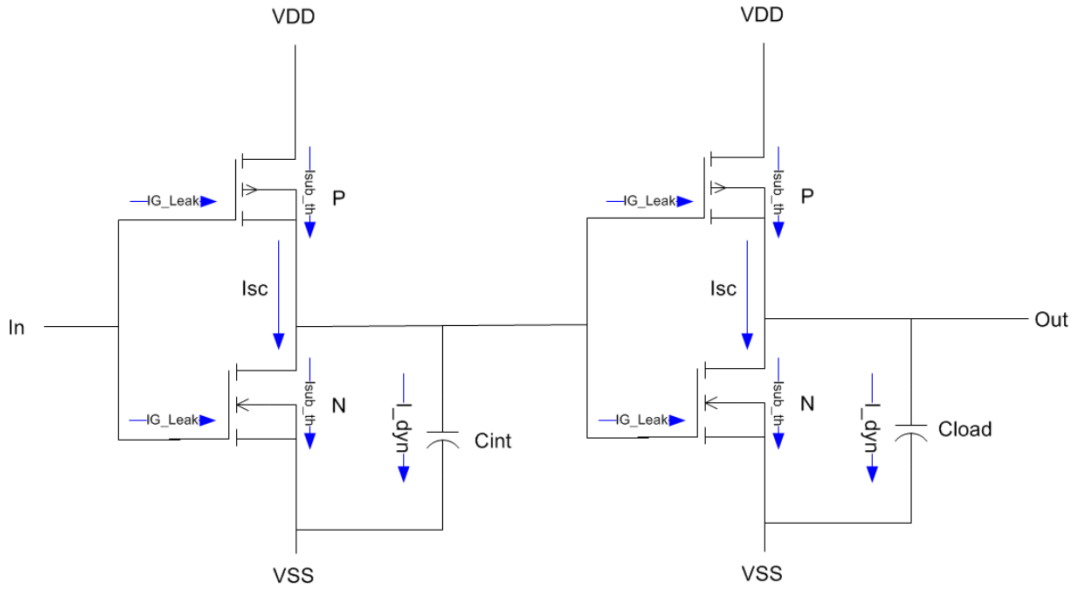
$P_{sc} : V_{dd}*I_{max}*((tr+tf)/2)* f$

Static (Leakage)

$P_{st} : V_{dd}*I_{sub\_th} + V_{dd}*I_{g\_leak}$

Total Power = $P_{dyn}+P_{sc}+P_{leak}$

- → Vdd @ 1.00V, relative power is 1
- → Vdd @ 0.75V, relative power is 0.56



- **CMOS still the most economic vehicle for complex MODEM and requires further detailed noise and power dissipation analysis.**

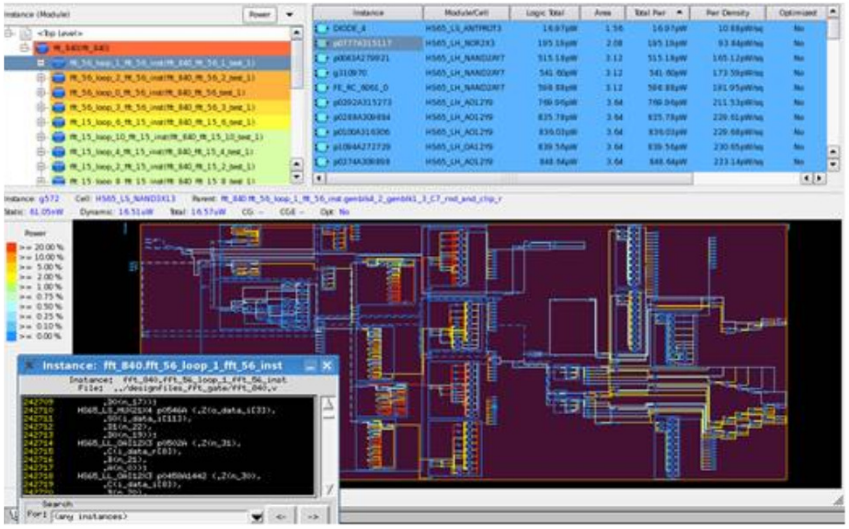
Process selection (Power estimations)

Spreadsheet Approach

+ Good for well known design and process

+ Easy to use and low cost

- Inaccurate results on new process with new library & IP



CAD Tool Approach

Half a dozen is on the market for power estimations based on gate or RTL VCD;

- Dedicated designer on the tool and costly

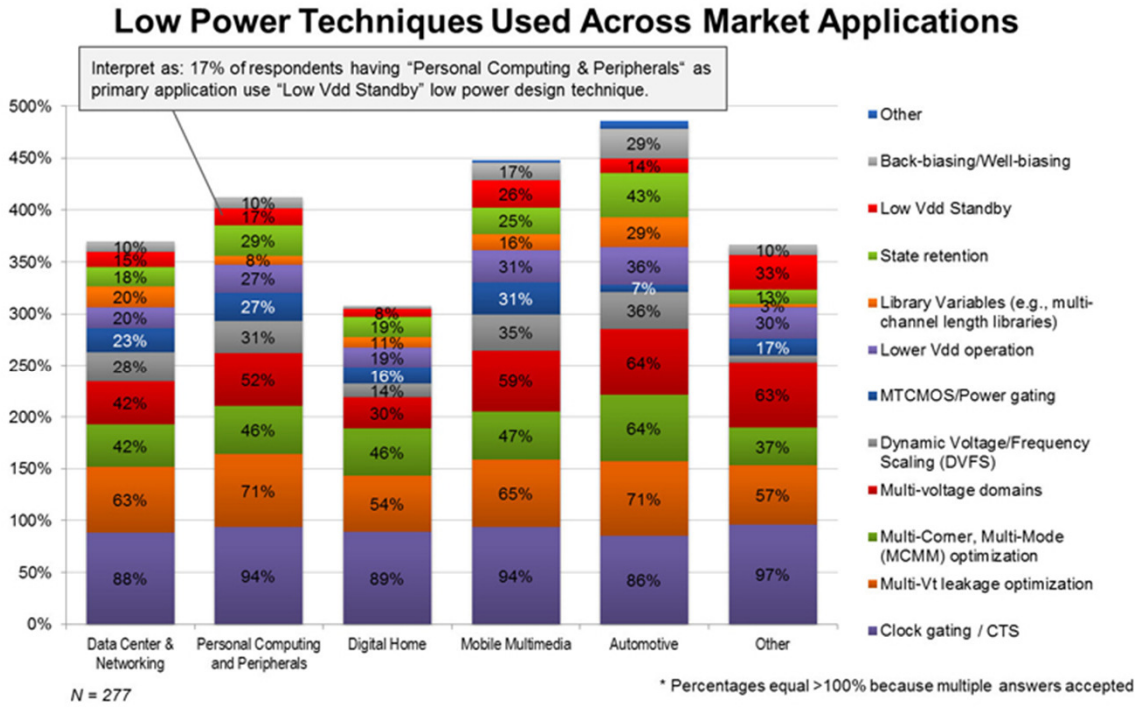
+ More accurate for new libraries if accuracy based on trial proven

1. Total power consumption

Power contribution				Power(Watts) Static	Dynamic	Total
Internal power						
Internal register power	79.7mW	641mW	721mW			
Internal latch power	0W	0W	0W			
Internal memory power	0W	0W	0W			
Other internal power	325mW	1.14 W	1.46 W			
Total internal power				404mW	1.78 W	2.19 W
IP Core power				0W	0W	0W
Pad power				0W	0W	0W
Clock power				25.3mW	382mW	407mW
Internal load power				0W	1.73 W	1.73 W
Total power				430mW	3.9 W	4.33 W

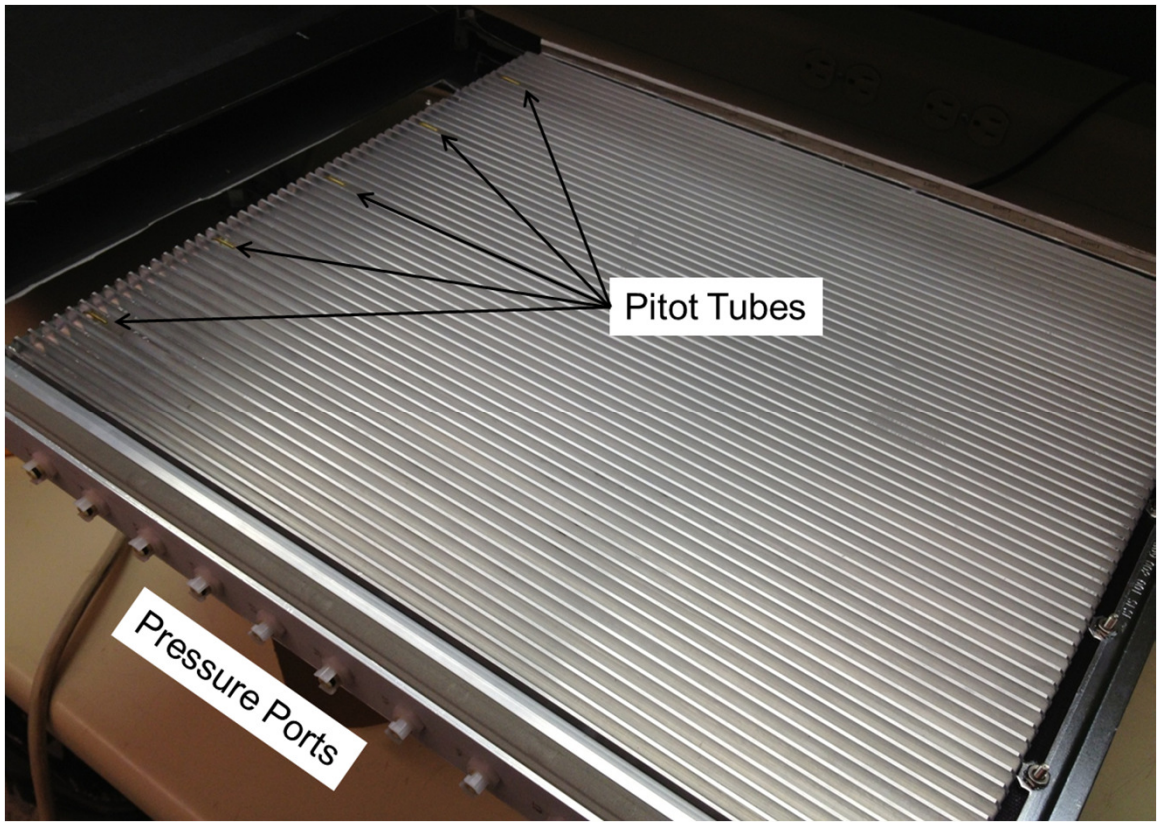
Efficiency for Silicon development

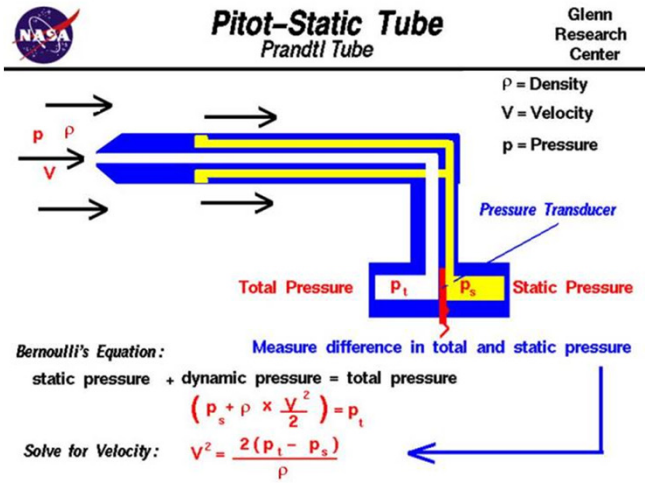
- This subject is maturing, but require a different architecture to reduce the carbon footprint in the Telecom industry.
- System developers should pressure ASIC development to use low power technics at the cost of "reasonable" schedule hit.



Source: Synopsys, Inc. Global User Survey, 2011

Conventional Fan – Where are we going?

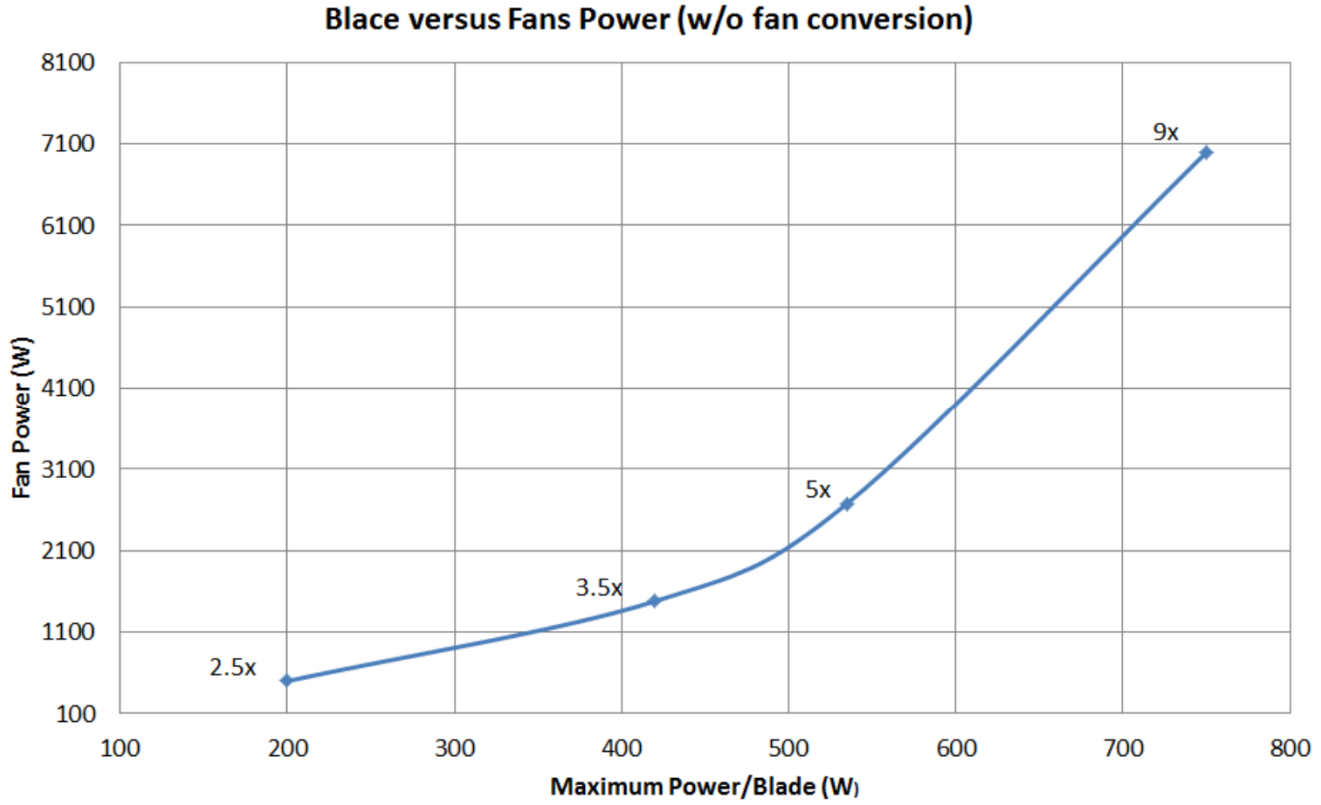




Fan just can’t keep up!

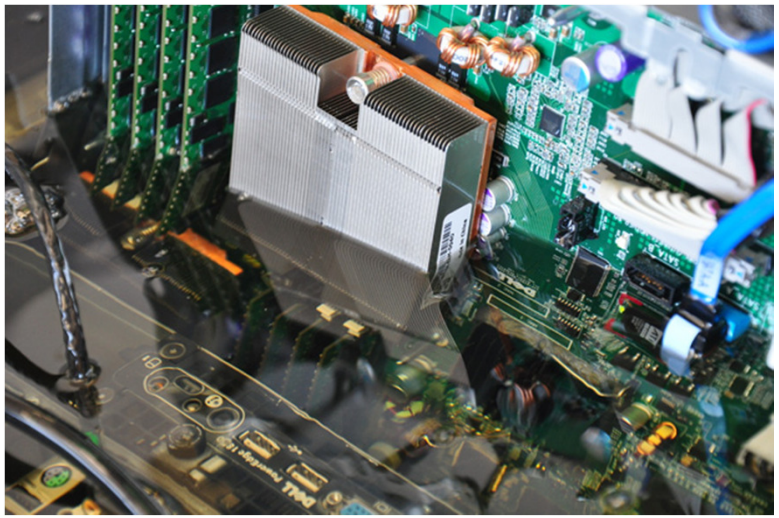
- **Conventional cooling stress the platforms and surtax power efficiency.**
- **Liquid cooling inevitable!**

*Measured at Fan input
**Assumes operation at 54ºC (50ºC ambient plus 4ºC for altitude compensation)
***Test Case: Switch analysis



Cooling Efficiency

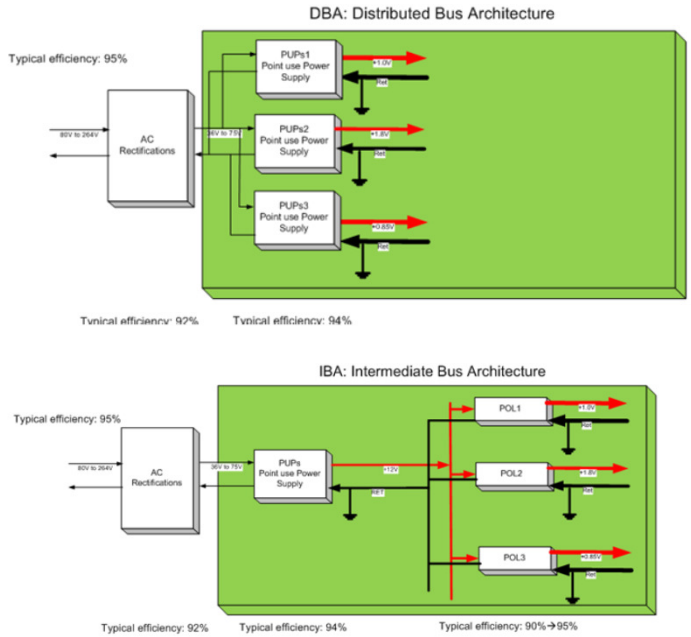
- **Blades approaches 3W/in^3 , and the limit, with forced air.**
- **Increased usage of Heat Pipes buys the industry time**
  - Not efficiency…
- **We have to use more efficient cooling mechanism in order to cool the hot spots like Liquid Cooling or "mineral oil" Immersion and use standard body to put pressure on the telecom industry.**



Courtesy of Green Revolution cooling

Power Supply Efficiency

Family Member Attribute	IBA	DBA
Total efficiency	77.5%	82.5%
Area	Medium	High
Hot Spots heatsinks	Good	Bad
Relative Costs	Medium	High



- **The selection of the power supply efficiency depends on the technology, platform and architecture.**
- **The industry requires to understand the requirement of large area, up to 40%, for power supply alone in a complex Transport architecture.**

Telecom Efficiency Figure of Merit

Alliance for Telecommunications Industry Solutions:

- Telecommunications Energy Efficiency Ratio, TEER, is only about a standard way of measuring and reporting measured data.

Energystar:

- Large Network Equipment Specification launched on October 2012 mostly targeted on Routers, Ethernet Switches, Security Appliances and Access Point Controllers.

Optical Transport next?

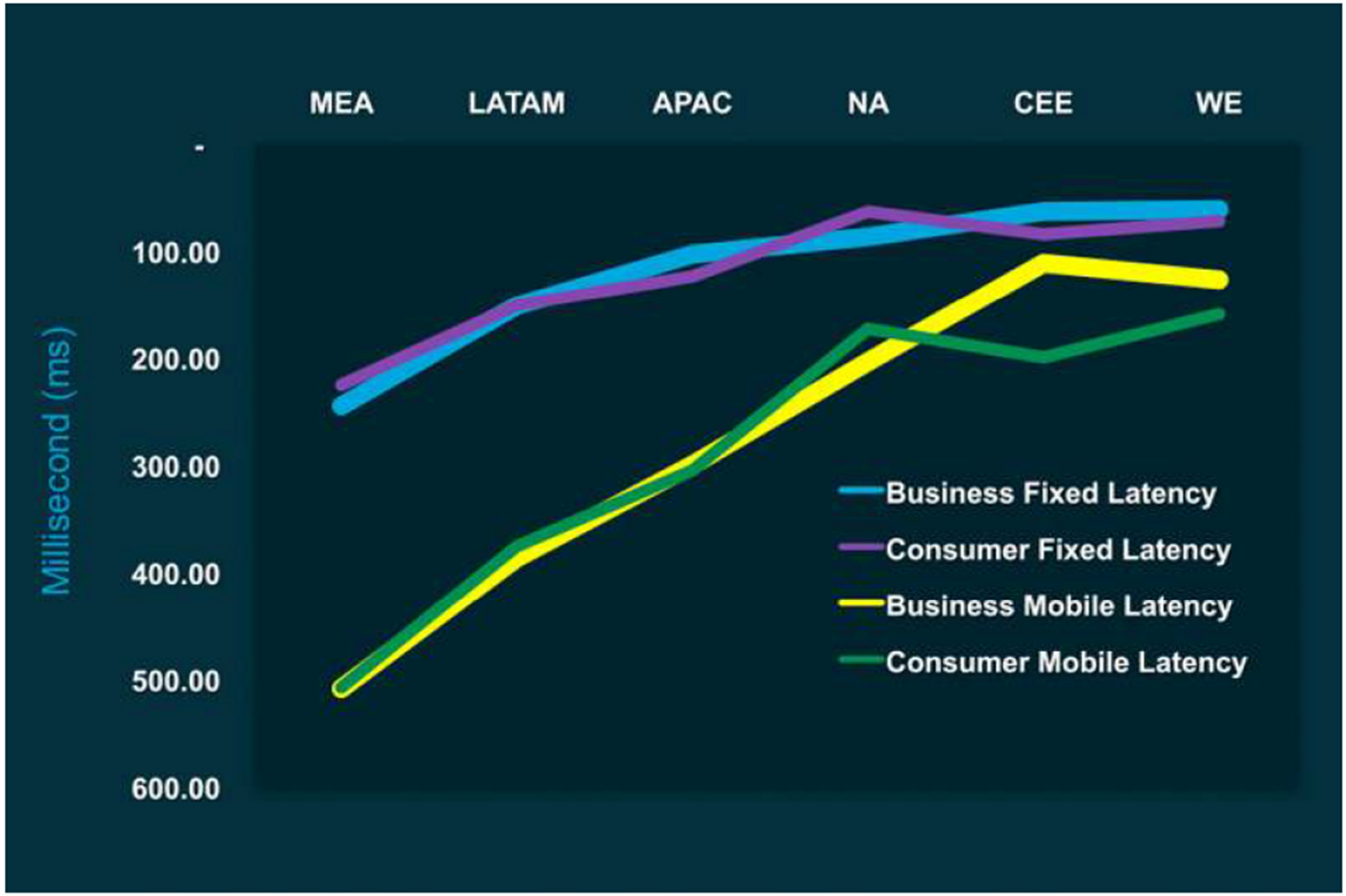
Conclusion

- **We don't pick the next generation because it's $0.7*P_n$!**
  - Use the selection procedure and tools available to select the proper CMOS process to your design constraints.
- **Liquid Cooling will soon reach Transport**
- **Success will be achieve via research collaboration, suppliers and customers**

Questions?

Appendix

Network Latencies by Region



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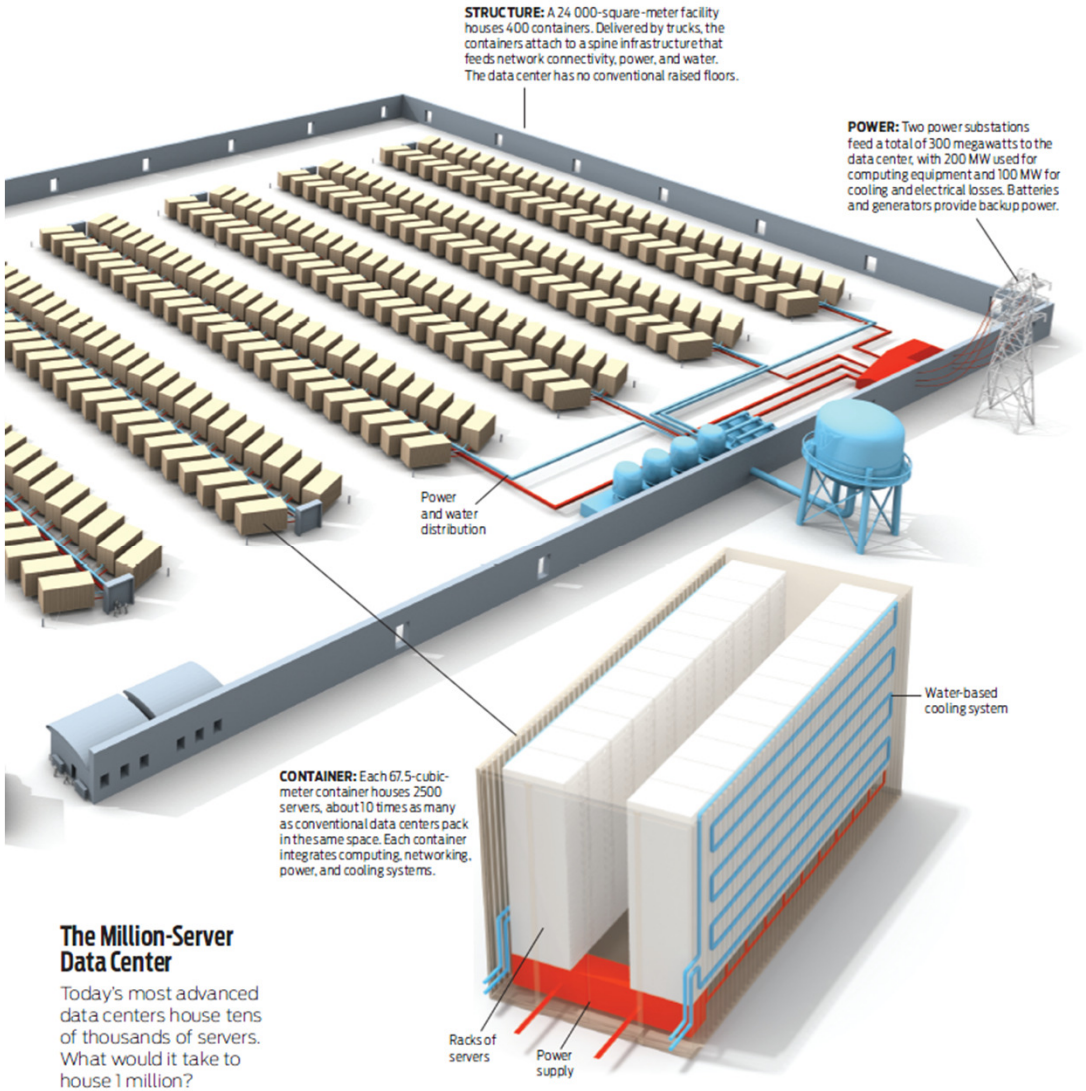
A Radical Change: Modular DCs

SELF-CONTAINED: Sun Microsystems' MD S20 is a standard shipping container housing eight racks of servers, storage systems, network gear, and power supplies [right]. The container's equipment consumes 187.5 kilowatts of power and uses a water-based cooling system [opposite].



The Million-Server Data Center

Today's most advanced data centers house tens of thousands of servers. What would it take to house 1 million?

- R. H. Katz, "Tech titans building boom," IEEE Spectrum, vol. 46, no. 2, pp. 40-54 , February 2009.

Geo-Distribution: Mega DC vs. Micro DC

- **Optimal placement and sizing:**
  - Redundancy and fault tolerance
  - Decrease propagation delays
  - Power, water, and fiber availability
  - Local policies: zoning, tax
  - Statistical multiplexing gains
  - Application types

- **Mega DC: 100,000s of servers (100,000s of square feet drawing10s of MW)**
- **Micro DC: 10,000s of servers**

❖ **K. Church, A. Greenberg, and J. Hamilton, "On delivering embarrassingly distributed cloud services,"Hotnets VII, October 2008.**