The GETB Project

Gigabit Ethernet Application Platform

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GETB Hardware

- Altera Stratix FPGA - 25000 logic elements
  - User code, 2 MAC “virtual” chips, PCI interface, 2 SDRAM controllers
- 2 Gigabit Ethernet ports (PHY chips)
- Memory:
  - 2 x 64 Mb SDRAM - packet descriptors, buffers
  - 2 x 512 kb SRAM - histograms, statistics
  - 2 Mbit on-chip memory in the FPGA
- 1 GPS clock input (clock synchronization between different cards)
- PCI 32bit @ 33MHz
- Flash memory

FPGA Firmware

- Most of the functionality: Handel-C
- Commercial IP cores for the MAC and PCI
- VHDL code used to connect logical entities
- Compiler (Fitter): Altera Quartus
  - Place & route tool: maps a logical circuit into gates (logic elements) in the FPGA
- Logic utilization: approx 85 - 90%
- Multiple clock domains: 41.6MHz (Handel-C), 125MHz (MAC), 33MHz (PCI), 10MHz (GPS)

Handel-C

- Hardware description language, like VHDL, but with syntax similar to C
- Contains built-in parallel constructs
  - The user can very easily write pieces of code that are executed in parallel (dedicated hardware is created for each parallel branch)
  - Synchronization primitives: channels, semaphores
- The result of the compilation is the description of an electrical circuit

Control software

- Entirely based on Python
- Distributed system –15 servers hosting 65 cards
- Server (having multiple GETB cards)
  - Linux OS with a custom kernel module
  - Python server application:
    - Configures the cards, updates 64bit counters
    - One thread per card handles remote client connections
- Client
  - Runs on any Python-compatible platform
  - Communicates to servers using an RPC protocol
  - Runs user scripts, displays statistics in a GUI

Traffic Generation (1)

- Based on packet descriptors created offline and loaded into SDRAM
  - Flexible way to specify any traffic distribution (Poisson, random, etc.)
- Multiple packet types: Raw Ethernet, IPv4, IPv6, special packets (VLAN, Flow-Control)
- All fields in the Ethernet and IP headers can be modified on a per-packet basis
- Works at Gigabit line-speed for all packet types
- Each packet contains:
  - Sequence number – for packet loss detection
  - Timestamp – to compute the one-way latency

Traffic Generation (2)

- Emulation of Atlas-like traffic (request-reply):
  - Physical ports are divided into clients and servers
  - Client ports send requests to server ports, asking for data
  - Replies from servers can have single or multiple frames (bursts)
  - Data rate is self tuned - clients can stop sending requests if not enough replies have been received
  - Emulates the traffic between fundamental Atlas applications: L2PU, SFI, ROS

Statistics

- Receiver keeps track of the following statistics for each remote source (in addition to global counters)
  - Packet loss
  - One way latency
  - Inter-packet Time (IPG)
- Histograms – they are stored into SRAM
  - Packets can be classified according to source or VLAN ID
  - Latency, IPG and packet size can be histogrammed
  - User defined resolution and histogram window (start offset, length)

Testing networking devices

- For each type of test a small Python script (function) is created to configure the system
- For each new device an interface is created that allows us to configure and get statistics from it using Python
- Several iterations over a given space of parameters are executed
  - Results and log files are saved automatically
  - After each iteration statistics from the tester are cross checked to those from the DUT
- The Device Under Test (DUT) can be any Layer 2 switch or Layer 3 router

Applications

- Three projects currently using the GETB
  - Gigabit Ethernet Tester
  - Network Emulator
  - Atlas ROB Emulator (an application that interacts directly to other Atlas software components)
- Other possible applications
  - Ethernet Sniffer (application that captures the traffic that is sent between its ports)