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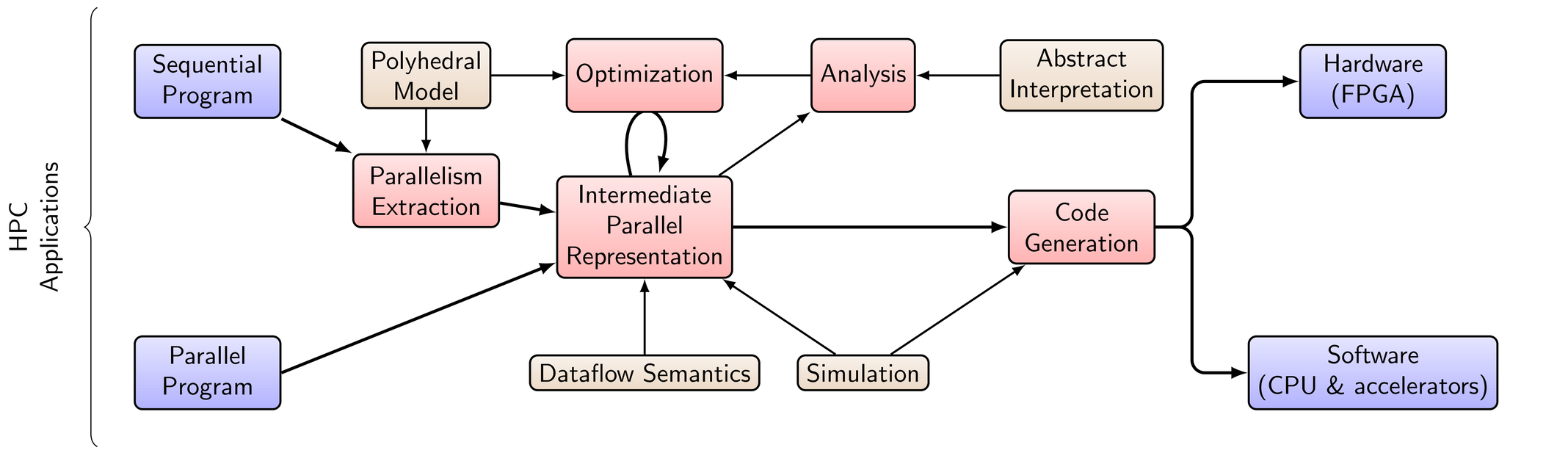
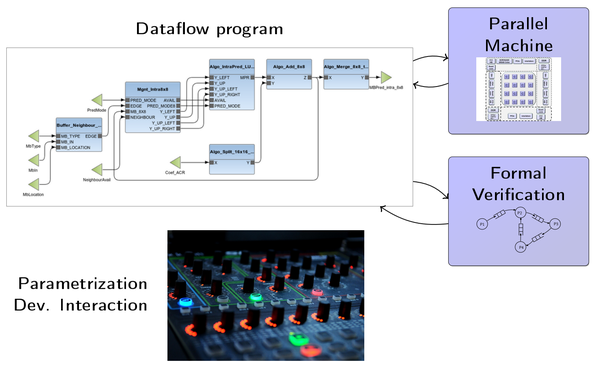
CASH
Compilation and Analysis, Software and Hardware

Analyses, Hardware/Software Compilation, Code Optimization for Complex Dataflow HPC Applications



Compiling and Scheduling Dataflow Programs



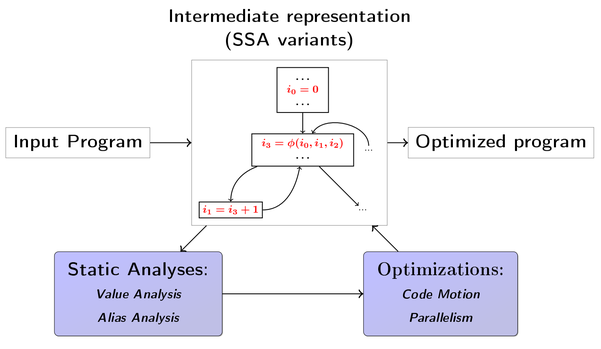
Locks:
- Different levels of granularities that do not coexist well
- What's the boundary between static and dynamic?

Added value:
- Combination of diverse formal reasoning on programs
- Collaboration with Kalray (Many-Core)

Short/Medium-term:
- Unify all kinds of parallelism in a same formal semantic framework
- Express compilation/analysis activities for this model
- Proof of concept, validation on literature examples (video algorithms, neural networks)

Long-term:
- Find suitable representations to compile from and to (intermediate representation + language)
- Implement a mature compiler infrastructure/toolbox

Scalable Static Analyses for General Programs



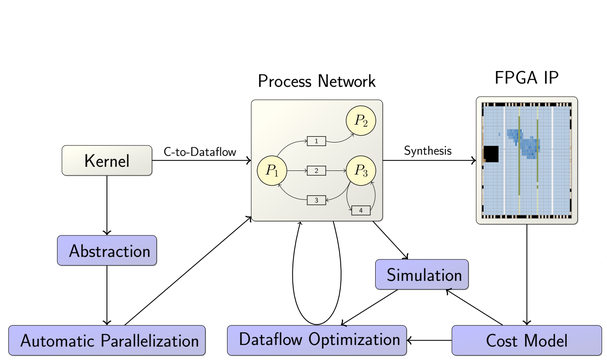
Locks:
- Classic abstract interpretation (AI) is too costly
- How to design optimization-oriented analyses
- Many syntax-based optimizations inside compilers

Added value:
- Experience on design and implementation of scalable analyses
- Cross-fertilization between compilation and abstract interpretation

Short/Medium-term:
- Rephrase/revisit syntax-based optimizations in the AI framework
- Revisit the polyhedral model optimizations
- Design new low cost analyses

Long-term:
- Find a theoretical framework (SSA-based?) to design scalable analyses
- Better interfaces for analyses and their optimization clients

Hardware Compilation for FPGA and Dataflow Optimization



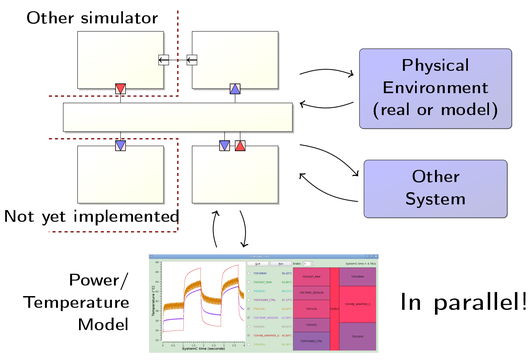
Locks:
- Energy budget & memory wall
- Classic automatic parallelization does not scale enough
- Dataflow analysis is hindered by dynamic control/data

Added value:
- Cross-fertilization high-level synthesis (HLS) / high-performance compilation
- Technological transfer to XtremLogic (Inria spin-off)

Short/Medium-term:
- Models and algorithms for data movement minimization
- Dataflow optimization for throughput and circuit surface
- Cost models for FPGA and fast simulation algorithms

Long-term:
- Lazy analysis and parametrization for scaling parallelization
- Abstraction and hardware for dynamic control/data

Simulation of Hardware



Locks:
- Heterogeneous simulation (functional + multi-physics, precise/abstract)
- Scale up ($\rightsquigarrow$ parallelism)

Added value:
- 15 years of collaboration w/ STMicroelectronics

Short/Medium-term:
- Convergence of approaches (CEA-LIST, LIP6...)
- Deal with loose information (intervals instead of individual values for physics)
- Application to simulation of data-aware process networks

Long-term:
- Framework for parallel and heterogeneous simulation: simulation backbone and adapters

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